DEPARTMENT OF COMMERCE

Bureau of Industry and Security

15 CFR Parts 734, 736, 740, 742, 743, 744, 748, 762, 772, and 774

[Docket No. 250108–0013]

RIN 0694–AJ98

Implementation of Additional Due Diligence Measures for Advanced Computing Integrated Circuits; Amendments and Clarifications; and Extension of Comment Period

AGENCY: Bureau of Industry and Security, Department of Commerce.

ACTION: Interim final rule, with request for comment.

SUMMARY: BIS is revising the Export Administration Regulations (EAR) in response to requests from the public to provide additional due diligence procedures regarding advanced computing integrated circuits (ICs). This interim final rule (IFR) will protect the national security of the United States and assist foundries and Outsourced Semiconductor Assembly and Test (''OSATs'') companies in complying with provisions of the EAR pertaining to advanced computing ICs in the supply chain. This IFR also revises the EAR to make amendments and clarifications to the EAR for changes made to the EAR in an IFR released by BIS on December 2, 2024, ''Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items,'' (FDP IFR), including extending the deadline for written comments for the FDP IFR to March 14, 2025.

DATES:

- *Effective date:* The effective date of this rule is January 16, 2025.
- *Compliance date:* Although this rule is effective January 16, 2025, exporters, reexporters, and transferors (in-country) are not required to comply with the new requirements of this rule until January 31, 2025. This compliance date only applies to EAR text that this rule revises, and does not otherwise impact any provision that was in effect prior to January 16, 2025 or added to the EAR through other rules. For example, under Export Control Classification Number (ECCN) 3A090, this IFR adds new Note 1 to 3A090.a, which, as new text, is subject to this compliance date. This IFR also revises ECCN 3A090.a. Only the new changes to ECCN 3A090.a in this particular rule are eligible for this compliance date.
- *Comment date:* Comments on this IFR must be received by BIS no later than March 14, 2025.
- *Extension of comment period for FDP IFR:* The comment period for the FDP IFR published December 5, 2024, at 89 FR 96790, is extended. Comments must be received on the FDP IFR by BIS no later than March 14, 2025.

ADDRESSES: Comments on this IFR, including the amendments and clarifications made for the FDP IFR described under section III.G of this IFR, may be submitted to the Federal rulemaking portal at: *www.regulations.gov.* The *regulations.gov* ID for this IFR is BIS–2024–0055. Please refer to RIN 0694–AJ98 in all comments.

All filers using the portal should use the name of the person or entity submitting the comments as the name of their files, in accordance with the instructions below. Anyone submitting business confidential information should clearly identify the business confidential portion at the time of submission, file a statement justifying nondisclosure and referring to the specific legal authority claimed, and provide a non-confidential version of the submission.

For comments submitted electronically containing business confidential information, the file name of the business confidential version should begin with the characters ''BC.'' Any page containing business confidential information must be clearly marked ''BUSINESS CONFIDENTIAL'' on the top of that page. The corresponding non-confidential version of those comments must be clearly marked ''PUBLIC.'' The file name of the non-confidential version should begin with the character ''P.'' Any submissions with file names that do not begin with either a ''BC'' or a ''P'' will be assumed to be public and will be made publicly available at: *https://www.regulations.gov.* Commenters submitting business confidential information are encouraged to scan a hard copy of the non-confidential version to create an image of the file, rather than submitting a digital copy with redactions applied, to avoid inadvertent redaction errors which could enable the public to read business confidential information.

FOR FURTHER INFORMATION CONTACT:

- For general questions, contact Regulatory Policy Division, Office of Exporter Services, Bureau of Industry and Security, U.S. Department of Commerce at 202–482–2440 or by email: *RPD2@bis.doc.gov.*
- For Category 3 technical questions, contact Carlos Monroy at 202–482–3246 or by email: *Carlos.Monroy@bis.doc.gov.*
- For Category 5 technical questions, contact Aaron Amundson at 202–482–0707 or *RPD2@bis.doc.gov.*

SUPPLEMENTARY INFORMATION:

I. Background

On October 7, 2022, BIS issued the first of a series of rules that restricted the ability of the People's Republic of China (PRC) and other countries of concern to obtain certain advanced computing ICs (*i.e.,* ICs exceeding specified performance thresholds) and related items (October 7 IFR). The controls in the October 7 IFR and the controls in the subsequent related rules were designed to prevent malicious state and non-state actors in the PRC and elsewhere from obtaining critical technology that they could use to threaten U.S. national security and foreign policy objectives. Today, through this IFR, BIS is updating the EAR to enhance the effectiveness of these controls. This IFR aims to address a common request from public comments on the October 7 IFR controls and subsequent related rules for more detailed guidance on how to conduct due diligence to confirm that an IC does not exceed the performance thresholds specified in EAR controls. In particular, this IFR focuses on providing ''front-end fabricators'' with objective, bright-line rules designed to assist in better identifying transactions with potential risk for diversion in a manner contrary to U.S. national security and foreign policy interests; enhancing due diligence procedures to ensure that new customers are appropriately vetted by ''front-end fabricators'' prior to providing ICs that may meet the advanced computing control levels; and improving reporting for transactions involving newer customers who may pose a heightened risk of diversion.

A. Semiconductors Are Central to the PRC's Technological and Military Ambitions

The PRC seeks to use advanced computing ICs and supercomputing capacity in the development and deployment of advanced computing systems and artificial intelligence (AI) models to further its goal of surpassing the military capabilities of the United States and its allies. Advanced or frontier AI capabilities such as large AI foundation models can lead to improved design and execution of weapons of mass destruction (WMDs), autonomous weapons, and advanced conventional weapons. Military decision-making aided by these AI models can improve

speed, accuracy, planning, and logistics. Advanced computing ICs are necessary for the development of these capabilities, because of the high processing power needed.

The use of advanced computing ICs in development and deployment of PRC AI models would further the PRC's goals of surpassing the military capability of the United States and its allies, a goal noted in the February 6, 2023, Annual Threat Assessment of the U.S. Intelligence Community (see *https://www.dni.gov/files/ODNI/documents/assessments/ATA-2023-Unclassified-Report.pdf*). That same report indicated that the PRC ''is rapidly expanding and improving its artificial intelligence (AI) and big data analytics capabilities, which could expand beyond domestic use,'' including to export its digital authoritarian ecosystem to assist in surveillance and to facilitate its transnational repression overseas.

Such activities by the PRC are contrary to U.S. national security and foreign policy interests as set forth in the Export Control Reform Act of 2018 (ECRA) (codified, as amended, at 50 U.S.C. 4801–4852), which directs BIS to control items subject to the jurisdiction of the United States when those items could be used in ''military programs that pose a threat to the security of the United States or its allies,'' could lead to ''the proliferation of weapons of mass destruction or of conventional weapons,'' or could undermine the ''foreign policy of the United States, including the protection of human rights and the promotion of democracy'' (50 U.S.C. 4811(2)).

B. Export Controls on Advanced Computing ICs

Accordingly, on October 7, 2022, BIS released the IFR, ''Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification'' (October 7 IFR) (October 13, 2022, 87 FR 62186), which amended the EAR to implement controls on certain ICs, computer commodities that contain such ICs, and certain semiconductor manufacturing items, and to make other EAR changes to implement appropriate related controls, including on certain ''U.S. person'' activities. The October 7 IFR explained that these controls were aimed at limiting the PRC's ability to engage in activities that would pose significant threats to U.S. national security and foreign policy. BIS determined that advanced computing ICs and related computing items—many of which originated in the United States or were produced with U.S. technology, software, or tools—could enable the PRC to develop certain enhanced data processing and analysis capabilities, including through AI applications because of the high processing power of the advanced computing ICs and related computing items.

Specifically, the October 7 IFR required a license for the export or reexport to the PRC of ICs and related items above a certain performance threshold (*e.g.,* those specified in Export Control Classification Number (ECCN) 3A090) that are the ''direct product'' of certain technology or software that is subject to the EAR or are produced by a plant or major component of a plant that is the direct product of such technology or software. That rule also imposed a license requirement for the export to certain entities on the Entity List of any items subject to the EAR that are the ''direct product'' of certain technology or software that is subject to the EAR or are produced by a plant or major component of a plant that is the direct product of such technology or software. This requirement significantly limited access to ''advanced-node integrated circuits (ICs)'' for the PRC, as production of ''advanced-node ICs'' requires U.S. technology, software, and tools. Exceeding the control thresholds for advanced computing ICs that were set in the October 7 IFR is extremely challenging without the use of U.S. technology, software, and tools, so controlling these items significantly reduced the PRC's ability to indigenously produce advanced computing ICs.

On October 25, 2023, BIS updated the controls imposed by the October 7 IFR to address advances in technology and ensure the controls remained effective. In particular, BIS learned that certain additional ICs could provide nearly comparable AI model training capability as those controlled in the October 7 IFR, and so further restricted those ICs. As such, the IFR, ''Implementation of Additional Export Controls: Certain Advanced Computing Items; Supercomputer and Semiconductor End Use; Updates and Corrections'' (AC/S IFR) (88 FR 73458, October 25, 2023), adjusted parameters for advanced computing ICs that are critical for advanced computing and AI applications, and imposed new measures to address the risk of circumvention of the controls, including expanding the license requirement for advanced computing ICs to apply to Country Groups D:1, D:4, and D:5.

In addition to the imposition of licensing requirements for advanced computing ICs and related items (*e.g.,* those specified in ECCN 3A090) to the PRC and elsewhere, BIS provided guidance through the AC/S IFR to help ensure that semiconductor foundries do not inadvertently violate the controls that are based on performance thresholds. Specifically, the AC/S IFR imposed a license requirement, including for transactions involving foreign produced items subject to the EAR pursuant to § 734.9(e)(2) (footnote 4), on 13 PRC entities involved in the development of advanced computing ICs by adding them to the Entity List. In addition, the AC/S IFR provided additional Red Flags and due diligence requirements to help ''front-end fabricators'' (*i.e.,* manufacturers of ICs designed by another party) identify whether IC designs meet the specified performance thresholds and thus require a license when destined for countries of concern. These Red Flags were designed to assist ''front-end fabricators'' to evaluate information provided by IC designers as to IC performance capabilities and assess whether foreign parties are attempting to circumvent controls by illicitly fabricating restricted ICs. In particular, Red Flag 19 gave producers of advanced ICs specific factors to identify a potential advanced computing IC regardless of a customer's assertion of an item's technical parameters. Specifically, it explained that if the item that would be produced is an IC, or a computer, ''electronic assembly,'' or ''component'' that incorporates more than 50 billion transistors and high bandwidth memory (HBM), it raises a Red Flag that there is a high degree of likelihood that a license is required under the EAR. Under standard BIS practice, when Red Flags are raised, the exporter, reexporter, or transferor (in-country) is required to investigate the circumstances and inquire about the end use, end user, or ultimate country of destination to resolve the Red Flag. If the Red Flag is not sufficiently resolved, then the exporter, reexporter, or transferor (in-country) should seek guidance from BIS by submitting an advisory opinion request to BIS or by submitting a license application to BIS.

On December 2, 2024, BIS released another IFR, ''Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items,'' (FDP IFR) (89 FR 96790, December 5, 2024), that made changes to the EAR controls for certain advanced computing items, supercomputers, and semiconductor manufacturing equipment, which includes adding new controls for certain

semiconductor manufacturing equipment and related items, creating new Foreign Direct Product (FDP) rules for certain commodities to impair the capability of certain destination or entities of concern to produce ''advanced-node ICs'', adding new controls for certain high bandwidth memory (HBM) important for advanced computing, and clarifying controls on certain software keys that allow for the use of items such as software tools. The FDP IFR published concurrently with another BIS final rule entitled, ''Additions and Modifications to the Entity List; and Removals from the Validated End-User (VEU) Program'' (Entity List rule) (89 FR 96830, December 5, 2024) that added to and modified the Entity List to ensure appropriate EAR controls are in place for certain critical technologies and to minimize the risk of diversion to entities of concern.

On January 13, 2025, BIS filed for public inspection, a rule related to this IFR, the ''Framework for Artificial Intelligence Diffusion'' IFR (AI Diffusion IFR) which imposed a worldwide regional stability (RS) license requirement for the export, reexport, or transfer (in-country) of advanced computing ICs classified under ECCNs 3A090.a, 4A090.a, and related .z items in § 742.6(a)(6)(iii)(A), and created several exceptions and pathways to authorization to facilitate transactions that pose a low risk of diversion or would otherwise advance U.S. national security or foreign policy interests, including U.S. technological leadership. Additionally, in January 2025, BIS filed for public inspection, a final rule related to this IFR, ''Additions to the Entity List'' (Foundry Entity List rule) which amends the EAR by adding 16 entities to the Entity List, under the destinations of China, People's Republic of (China) (14) and Singapore (2).

C. National Security Basis for Additional Controls Related to ''Applicable Advanced Logic Integrated Circuits (ICs)''

Following the implementation of the October 7 IFR in 2022, BIS has continued to study and assess the effectiveness of its controls in protecting U.S. national security and foreign policy interests. In so doing, BIS has relied on open-source reporting, public comments, industry analysis, and other sources of information available to the U.S. Government.

Over the past year, BIS determined that modifications to existing controls are warranted. BIS assessed that relevant Entity List entries, Red Flag requirements and technical guidance have not fully ensured that foundries producing ICs for IC designers and other related companies in the IC supply chain are able to definitively determine whether those ICs meet or exceed the ECCN 3A090 control parameters. As noted above, the EAR provides a series of Red Flag indicators that foundries can use to assess an IC's performance level. However, BIS has assessed that entities seeking to divert ICs that meet the control parameters of ECCN 3A090 to unauthorized end uses and end users may misrepresent the performance capabilities of their ICs in a manner that would make it difficult for a foundry to adequately verify the performance of such items. As an initial matter, BIS has assessed that ICs with a transistor count below that specified in current Red Flag 19 (50 billion) can meet the performance threshold specified in ECCN 3A090. The Red Flag thus provides no guidance to foundries that receive orders for ICs with transistor counts below 50 billion in verifying their customers' assertions that those ICs do or do not fall within ECCN 3A090.

Furthermore, these technical challenges in assessing the performance of an IC can emerge at multiple stages of the IC production process. In cases where a foundry does not control the final packaging of an IC, ICs are at risk of being diverted and later packaged into products that exceed the performance thresholds set out in ECCN 3A090. For example, a customer may request an IC with a transistor count just below the current transistor count Red Flag threshold, and contract with an OSAT company to incorporate that IC into a packaged item that exceeds the performance thresholds specified in ECCN 3A090. Such challenges in assessing the ultimate performance capabilities of an IC create a heightened risk that a foundry will fail to detect efforts by third parties to evade BIS controls.

Even in cases where a foundry retains control over a wafer through packaging and testing, BIS has identified challenges in ensuring compliance with advanced computing IC controls. BIS understands that contractual arrangements could prohibit foundries from analyzing certain business confidential information (*e.g.,* a design file) that would give greater clarity into an IC's ultimate usage and performance capabilities. Additionally, it can be challenging to assess the performance of an IC based on a design file. This lack of visibility into IC performance means such ICs may exceed ECCN 3A090 performance thresholds and ultimately be diverted to the PRC and other destinations of national security concern or prohibited entities for use in advanced AI applications. BIS has therefore assessed that controls would be more effective with verifiable technical metrics such as node, which is immediately verifiable by the foundry, and transistor count, which is verifiable through communication between foundry and OSAT.

The risk that an IC designer might misrepresent the ECCN of ''applicable advanced logic ICs'' that meet the control parameters of ECCN 3A090 and divert these ICs to unauthorized end uses or end users is not hypothetical. BIS has observed persistent efforts to evade the controls on ''advanced computing ICs,'' as well as restrictions imposed through the Entity List, by the PRC and other entities through intermediaries and/or shell companies. Open-source reporting described PRC companies using foreign subsidiaries or other means to purchase ICs subject to EAR controls. To counter these efforts, as well as PRC operations inside and outside of the PRC (including the Hong Kong and Macau Special Administrative Regions as specified in the EAR) seeking to acquire advanced computing ICs through transshipment, diversion, and accessing datacenters with advanced computing ICs in destinations across the world, the AC/S IFR and the AI Diffusion IFR expanded the scope of destinations for which a license is required to export, reexport, or transfer (in-country) advanced computing ICs.

Although BIS's controls have been effective, they have not entirely prevented the diversion of advanced computing ICs to the PRC and other destinations and entities of concern. Accordingly, BIS has determined that further restrictions on these ICs are warranted to ensure that advanced computing ICs are only exported to customers with low risk of diversion to restricted entities. While certain IC designers and/or OSATs have a long history of compliance with export controls, more safeguards are needed to ensure that the PRC and other entities cannot access advanced computing ICs through diversion from third parties.

To that end, this IFR imposes a broader license requirement for ''front-end fabricators'' and ''OSAT'' companies seeking to export, reexport, or transfer (in-country) certain ''applicable advanced logic integrated circuits'' under ECCN 3A090.a to or within any destination worldwide (see § 742.6(a)(6)(iii)(A) of the EAR, which works in conjunction with new Note 1 to 3A090), unless the license requirement is overcome in any of the three ways outlined in paragraphs a. through c. of Note 1 to 3A090. To

exclude the substantial number of low-risk transactions potentially captured within this expanded scope, the rule provides three ways to overcome the license requirement and creates lists of reliable sources to verify technical parameters of ''applicable advanced logic ICs:''

(i) Approved IC designers (listed in supplement no. 6 to part 740),

(ii) Approved ''OSAT'' companies (listed in supplement no. 7 to part 740), as well as

(iii) A method of identifying authorized IC designers with criteria included in Note 1 to 3A090.a.

Approved listed entities are those that submit requests to BIS to be added to a list and are approved through the End-user Review Committee (ERC) to be added to the relevant list. (see section III.D for the description of the criteria used in making such decision as specified in § 748.16(a)(4) and section III.B).

Authorized IC designers are those that meet the criteria under new Note 1 to 3A090.a. Prior to April 13, 2026, authorized IC designers include all IC designers that are headquartered in Taiwan or a destination specified in Country Group A:1 or A:5, that are neither located in nor have an ultimate parent headquartered in Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR; and that have agreed to submit applicable information described in § 743.9(b) to the ''front-end fabricator,'' which the ''front-end fabricator'' must then report to BIS. After April 13, 2026, authorized IC designers include any IC designer that both meets those criteria and has submitted an application to become an approved IC designer. However, any company deemed an authorized IC designer after April 13, 2026, will cease to be an authorized IC designer 180 days after the submission of its application to become an approved IC designer.

This rule also modifies License Exceptions Artificial Intelligence Authorization (AIA) and Advanced Compute Manufacturing (ACM) so that certain exceptions are only available for items designed by approved IC designers who are likely to accurately report the ECCN of the items they request advanced foundries to fabricate.

II. Overview of This Interim Final Rule

In this IFR, BIS makes changes to EAR controls in seven categories. The six categories of changes implemented by this IFR are described in section III as follows:

A. Revises License Exceptions AIA and ACM;

B. New supplement nos. 6 and 7 to part 740, including lists of approved IC designers and approved ''OSAT'' companies, as well as authorized IC designers in specified destinations;

C. New reporting requirements for ''front-end fabricators'' producing advanced computing ICs for authorized IC, as well as a new ''Know Your Customer'' (KYC) vetting form;

D. Application process for additions, modifications, and removals from the approved IC designer and approved ''OSAT'' company lists;

E. New Definitions;

F. Revisions to ECCNs to clarify scope of ECCN 3A090; *and*

G. Amendments and clarifications to the EAR as set forth in the FDP IFR.

III. Changes to the EAR

A. Revisions to License Exceptions Artificial Intelligence Authorization (AIA) and Advanced Compute Manufacturing (ACM)

This IFR revises the items within the scope of two license exceptions: License Exception AIA (§ 740.27) and License Exception ACM (§ 740.28). License Exception AIA authorizes the export, reexport, and transfer (in-country) of the items identified in paragraphs (a)(1) and (a)(2) to entities located within destinations listed in paragraph (a) of supplement no. 5 to part 740, unless the entity is headquartered outside of, or has an ultimate parent company headquartered outside of, a destination specified in paragraph (a) of supplement no. 5 to part 740, with an expanded authorization for certain model weights in paragraph (a)(3), subject to additional conditions. License Exception ACM authorizes the export, reexport, and transfer (in-country) of eligible items (ECCNs 3A090, 4A090, and related .z commodities, software, and technology) to a 'private sector end user' that is located in a destination not listed in Country Group D:5 or Macau, provided it is not headquartered in and does not have an ultimate parent company headquartered in Macau or a destination specified in Country Group D:5, if the ultimate end use is the ''development,'' ''production'' or storage (in a warehouse or other similar facility) of such eligible items.

This IFR amends License Exception AIA by adding a requirement for three of the eligible commodities for this exception: ECCNs 3A090.a; 5A002.z.1.a, z.2.a, z.3.a, z.4.a, z.5.a; and 5A992.z.1. The requirement for those three ECCNs provides that those ECCNs are eligible for this license exception only if they are designed by an approved or authorized IC designer, as described in supplement no. 6 to part 740 and Note 1 to ECCN 3A090.a, respectively. This requirement is intended to ensure that foundries and other entities seeking to use this exception can do so only if the items have been designed by an entity that presents a low risk of diversion. As provided in Note 1 to ECCN 3A090.a, authorized IC designers are those that are (i) in Taiwan or a location specified in Country Group A:1 or A:5, that are neither headquartered nor have an ultimate parent headquartered in Macau or a location specified in Country Group D:5 of supplement no. 1 to part 740 and (ii) for whom transactions are subject to the reporting requirements in § 743.9 of the EAR.

This IFR similarly revises License Exception ACM. Paragraph (b) is revised by adding a requirement for three of the eligible commodities for this exception: ECCNs 3A090.a; 5A002.z.1.a, z.2.a, z.3.a, z.4.a, z.5.a; and 5A992.z.1. The requirement for those three ECCNs provides that those ECCNs are eligible for this license exception only if designed by an approved or authorized IC designer, as described in supplement no. 6 to part 740 and Note 1 to ECCN 3A090.a, respectively. As with the new requirement for License Exception AIA, this requirement is intended to ensure that foundries and other entities seeking to use License Exception ACM can do so only if they are working with entities that pose a low risk of diversion.

These revisions ensure License Exceptions ACM and AIA authorization for these three ECCNs are only available when designed by approved or authorized IC designers, which supports the more secure supply chain. The EAR still requires ''front-end fabricators'' to conduct continuous technical and KYC due diligence for authorized and approved IC designers and report their results to BIS. This ensures BIS has up-to-date information on these entities, enabling BIS to act on any concerning information reported. The factors used to designate authorized and approved IC designers are discussed in more detail below, but entities determined to have a strong history of export control compliance and that have been vetted by the U.S. government are likely to be trustworthy IC designers. Additionally, these exceptions are available for items designed by authorized IC designers headquartered in countries A:1, A:5, and Taiwan, which are destinations that are members of multilateral export control regimes (*e.g.,* the Wassenaar Arrangement on Export Controls for Conventional Arms and Dual-use Goods and Technologies), have the authority to control key items of concern, or otherwise have incentive to ensure

compliance with these additional requirements. These destinations share the U.S. government's interest in countering diversion or misuse of advanced node ICs and promoting mutual security, and companies in such destinations will generally have a lower likelihood of misrepresenting the technical specifications of their items to advanced foundries.

Based on the changes in this IFR, these amended license exceptions will facilitate low-risk trade while allowing the U.S. government to vet prospective approved entities for such advanced ICs in the first instance, rather than relying solely on foundry due diligence to identify potential diversion risks. The reporting requirements associated with authorized IC designers will also allow the U.S. government visibility into the verification process between these entities and the advanced foundries to assure that it is operating as envisioned. It will therefore become much more difficult for entities headquartered in Macau or destinations specified in Country Group D:5 to obtain advanced computing ICs subject to the EAR by attempting to place orders through entities that might misrepresent the technical specifications of their items and then divert advanced computing ICs to restricted destinations.

B. New Supplement Nos. 6 and 7 to Part 740, Including Lists of Approved IC Designers and Approved ''OSAT'' Companies, as Well as Authorized IC Designers

Part 740 is amended by adding supplement nos. 6 and 7 to create two new lists of entities: approved IC designers (supplement no. 6) and approved ''OSAT'' companies (supplement no. 7).

In deciding which entities to initially include in these supplements, the agencies represented on the End User Review Committee (ERC) have assessed a variety of national security and foreign policy factors, including the company's record of engagement in appropriate end-use activities; the company's export licensing and related history indicating compliance with U.S. export controls and existence of other potential derogatory information related to said company (*e.g.,* information raising questions about ownership of the company); whether the applicant has a longstanding history of advanced IC purchases; the ability of the applicant to guard against both the misuse and diversion of computing resources; the location of the company's headquarters and its principal place of operations; the volume and nature of the company's trade in ICs; and other factors as determined by BIS to be relevant. In deciding on which entities warrant inclusion or removal from these supplements, the ERC will apply the same factors.

i. Addition of supplement no. 6 to part 740.

New supplement no. 6 to part 740, which is referenced in the Note 1 to ECCN 3A090.a, lists as approved IC designers Advanced Micro Devices, Inc., Alphabet Inc., Amazon.com, Inc., Analog Devices, Inc., Apple Inc., BAE Systems, Inc., Block, Inc., The Boeing Company, Broadcom Inc., Cerebras Systems Inc., Cisco Systems, Inc., Hewlett Packard Enterprise Company, Honeywell International, Inc., Infineon Technologies AG, Intel Corporation, International Business Machines Corporation (IBM), L3Harris Technologies, Inc., Marvell Technology, Inc., MediaTek Inc., Meta Platforms, Inc., Micron Technology, Inc., Microsoft Corporation, Mitsubishi Group, Nokia Corporation, Nvidia Corporation, NXP Semiconductors N.V., Qualcomm Incorporated, Raytheon Company, Realtek Semiconductor Corporation, Sony Group Corporation, Tesla, Inc., Texas Instruments, *and* Western Digital Technologies, Inc. Section 748.16 explains how to apply to be added to the list of approved IC designers. To be added to the list of approved IC designers, an IC designer with plans to produce one or more ICs classified under ECCN 3A090.a must submit to BIS a request in the form of an advisory opinion that is accompanied by certain required information, *i.e.,* the information in new supplement no. 4 to part 748. The processing of advisory opinion requests to add companies to the approved IC designer list in supplement no. 6 to part 740 will follow the interagency process for review of Validated End-User requests set forth in supplement no. 9 to part 748 of the EAR. BIS will conduct supplemental outreach to the companies initially included in supplement no. 6 to part 740 to ensure continued compliance with the EAR, including the requirements promulgated by this IFR.

ii. Addition of supplement no. 7 to part 740.

Supplement no. 7 to part 740 lists the following companies as approved ''OSAT'' companies, which is referenced in the Note 1 to ECCN 3A090.a: Amkor Technology, Inc., Ardentec Corporation, ASE Technology Holding Co., Ltd., Doosan Tesna Inc., Fabrinet, Giga Solution Tech. Co., Ltd., GlobalFoundries, Inc., HT Micron Semicondutores SA, Intel Corporation, International Business Machines Corporation (IBM); KESM Industries Berhad, LB Semicon Inc. Micro Silicon Electronics Co., Ltd., Nepes Corporation, Powertech Technology Inc (PTI), QP Technologies, Raytek Semiconductor, Inc., Samsung Electronics Co. Ltd., SFA Semicon, Shinko Electric Industries Co. Ltd., Sigurd Microelectronics Corporation., Steco Co., Ltd., Taiwan Semiconductor Manufacturing Company Limited (TSMC), and United Microelectronics Corporation (UMC). To develop this list, BIS identified ''OSAT'' companies currently engaged in production of ''applicable advanced logic ICs'' headquartered outside of Macau or locations specified in Country Group D:5 in supplement no. 1 to part 740 of the EAR. BIS and the other export control agencies then vetted these entities on a case-by-case basis. Based on a review of open source and other information available to the U.S. Government, these companies have been determined to be approved. Therefore, these companies' attestations regarding the ''aggregated approximated transistor count'' of a final, packaged item can be used to overcome the presumption in Note 1 to ECCN 3A090.a that an ''applicable advanced logic integrated circuit'' is a 3A090.a item.

To apply to be added to the list of approved ''OSAT'' companies, § 748.16 specifies that an ''OSAT'' company with plans to test, assemble, or package one or more items exceeding the technical thresholds of 3A090.a designed by the approved IC designer must submit a request in the form of an advisory opinion to BIS. The processing of advisory opinion requests to add companies to the approved ''OSAT'' company list in supplement no. 7 to part 740 will follow the interagency process for review of Validated End-User requests set forth in supplement no. 9 to part 748 of the EAR.

BIS will conduct supplemental outreach to the companies initially included in supplement no. 7 to part 740 to ensure continued compliance with the EAR, including the requirements promulgated by this IFR.

C. Reporting Requirements for ''Front-End Fabricators'' Producing ''Applicable Advanced Logic Integrated Circuits'' for Authorized IC Designers

Section 743.9 adds new reporting requirements for ''front-end fabricators'' producing any IC specified in ECCN 3A090.a for authorized IC designers. Authorized IC designers are those that meet the criteria under new Note 1 to 3A090.a., including having agreed to submit applicable information described in § 743.9(b) to the ''front-end fabricator,'' which the ''front-end

fabricator'' must then report to BIS and excludes these entities from some of these license requirements as described in Note 1 to 3A090.a. These new reporting requirements are designed to ensure the U.S. government has visibility into companies that are not listed on the initial approved IC designer list.

Note that BIS continuously monitors export licensing and trade data, and may take corrective action, including the imposition of reporting requirements, with respect to approved ''OSAT'' companies and approved IC designers should such parties present U.S. national security or foreign policy concerns.

Paragraph (a) to § 743.9 stipulates that reports must be submitted to BIS in accordance with this section by ''front-end fabricators'' producing ICs specified in ECCN 3A090.a for any authorized IC designers (§ 743.9(a)). Because only a small number of ''front-end fabricators'' are capable of producing ICs specified in ECCN 3A090.a, this allows for consolidation of reporting requirements from the smaller set of ''front-end fabricators,'' who can help to verify the much wider sets of IC designers and ''OSAT'' companies they work with. Structuring the reporting requirement for ''front-end fabricators'' ensures that the economic and compliance burden is minimal and placed on the companies who are best positioned to provide information that can help address potential diversion concern. Additionally, ''front-end fabricators'' need not provide information about exports, reexports, or transfers (in-country) to an entity that is an authorized IC designer and becomes an approved IC designer.

Paragraph (b) to § 743.9 identifies the information that must be collected by the ''front-end fabricator'' and included in each report to BIS regarding authorized IC designers (*e.g.,* the name, address, and point of contact of the authorized IC designer; the end-user vetting form included in supplement no. 2 of this part; and a description of each category of IC specified or presumed to be specified under ECCN 3A090.a sold during the reporting quarter). The information in the report about the IC specified or presumed to be specified under ECCN 3A090.a should include the designer, product names, model number (if known), and quantity sold during the reporting quarter. This information provides the U.S. government visibility over the verification process.

The final three paragraphs of § 743.9 provide more information on how to submit reports, and where to submit general information on reporting. Paragraph (c)(1) to § 743.9 establishes that reports must be submitted on a quarterly subject to the provisions of this section, and that the first report must be submitted by May 31, 2025 and the report shall cover any exports, reexports, and transfers (in-country) during the time between January 31 and April 30, 2025. Thereafter, paragraph (c)(2) states that reports for the reporting period ending April 30 must be received by BIS no later than May 31. Reports for the reporting period ending July 31 must be received by BIS no later than August 31. Reports for the reporting period ending October 31 must be received by BIS no later than November 30. Reports for the reporting period ending January 31 must be received by BIS no later than February 28. Paragraph (d) provides the email address, *EAR.Reports@bis.doc.gov,* where reports must be submitted with authorized IC designer in the subject line. Paragraph (e) notes that general information or questions about the reports can be submitted to the Office of National Security Controls, Tel. (202) 482–0092, or Email: *EAR.Reports@bis.doc.gov.*

The authorized IC designer KYC Vetting Form discussed in § 743.9 has been added through this IFR in new supplement no. 2 to part 743. This supplement contains a questionnaire that must be completed as part of the reporting requirements for authorized IC designers in § 743.9 of the EAR. Unresolved answers of ''Yes'' to questions in the form in supplement no. 2 to part 743 are considered a Red Flag. The ''front-end fabricators'' would need to conduct additional due diligence before proceeding with the transaction. The questions in the form are KYC best practices that are especially critical in this context where there is a risk of companies seeking advanced foundry services in circumvention of controls on advanced computing items. They are not an exhaustive list of due diligence requirements but provide important information that should be part of KYC screening. These questions focus on three areas: the legitimacy of the authorized IC designer; whether the authorized IC designer matches any entry on the Consolidated Screening List; and screening of any other parties to a given transaction; and general Red Flags such as whether a freight forwarding firm is listed as the final destination or whether any party appears to be overpaying for a transaction.

D. Application Process for Additions, Modifications, and Removals From the Approved IC Designer and Approved ''OSAT'' Company Lists

i. Changes to the advisory opinion process being used to request being added, modified, or removed from the lists of approved IC designers or approved ''OSAT'' companies.

In § 748.3(c) (Advisory opinions), this IFR makes revisions to account for the advisory opinion process that will be used to request a party to be added, removed, or modified from the list of approved IC designers in supplement no. 6 to part 740 or approved ''OSAT'' companies in supplement no. 7 to part 740. Those changes are implemented in paragraph (c)(4) of § 748.3. This IFR redesignates existing paragraph (c)(4) as paragraph (c)(5).

ii. Section 748.16: Application for additions and modification to, or removals from the list of approved IC designers and approved ''OSAT'' companies.

Part 748 is amended by adding new section § 748.16 for addition, removal, or modification requests for approved IC designers and approved ''OSAT'' companies. To be eligible to be listed in supplement no. 6 or 7 to part 740 of the EAR, § 748.16 notes that applicants must adhere to the provisions set forth in paragraphs (a) through (d) of this section. These provisions, discussed in greater detail in the paragraphs below in this section III.D.ii, establish eligibility for approved IC designer and approved ''OSAT'' company status, create protocols for additions, modifications, and removals from the list of approved IC designers and ''OSAT'' companies. Section 748.16 notes that if a request to be listed in supplement no. 6 or no. 7 to part 740 of the EAR is not granted, no new license requirement is triggered. In addition, such a result does not render the entity ineligible for license approvals from BIS, nor does it preclude the subsequent approval of a request to be listed in supplement no. 6 or 7 to part 740. These clarifications are to ensure an entity is not dissuaded from applying to be listed in this supplement.

Paragraph (a)(1) to § 748.16 states that only entities that have designed, assembled, tested, or packaged ICs, or have credible plans to do so, will be considered for addition to either list in supplement no. 6 or 7 to part 740. Entities headquartered or having an ultimate parent headquartered in Macau or a destination in Country Group D:5 are not eligible, as they are at risk of facing significant pressure to provide inaccurate information to the ''front-end fabricators'' in order to gain access to

advanced foundry services to make restricted advanced ICs. Meanwhile, entities that have not designed, assembled, tested, or packaged ICs and have no credible plans to do so are not eligible for inclusion on either list since they cannot attest to the performance specifications of ICs they have not designed, assembled, tested, or packaged themselves.

Paragraph (a)(2) provides a requirement to include, with a request for addition to a list, the information in supplement no. 4 to part 748. The information in this required supplement is much like the information required of Validated End User (VEU) applicants (*i.e.,* identity, ownership, methodology for recordkeeping, certification of compliance with all the provisions of § 748.16, and a statement of acknowledgement and agreement).

Paragraph (a)(3) provides an email address to send all types of requests. Requests must be submitted in the form of an advisory opinion request, as described in § 748.3(c), and requests should be marked ''approved supply chain entities request'' and emailed to *approved_supply_chain@bis.doc.gov.*

Paragraph (a)(4) establishes some of the factors used by the End-User Review Committee (ERC) in evaluating an applicant for eligibility to be listed as an approved IC designer or approved ''OSAT'' company. The factors include: (i) the applicant's record of exclusive engagement in appropriate end-use activities; (ii) the applicant's compliance with U.S. export controls; (iii) the need for an on-site review prior to approval; (iv) the applicant's capability of complying with the requirements of being listed as an approved IC designer; (v) the ability of the applicant to guard against both the misuse and diversion of computing resources; and (vi) the applicant's relationships with U.S. and foreign companies. In addition, subparagraph (a)(4) states that when evaluating the eligibility of an IC designer or ''OSAT'' company for approved status, the ERC will consider the status of the export controls of the country or countries where the applicant is headquartered, and these countries' support of and adherence to multilateral export control regimes. All of these factors are relevant to assessing the risk that an applicant will adhere to all U.S. export control regulations and poses a low risk of diversion.

Next, paragraph (a)(5) notes that listings of approved IC designers, and approved ''OSAT'' companies are subject to revision, suspension, or revocation entirely or in part, and paragraph (a)(6) emphasizes that information submitted in an addition or modification request is deemed to constitute continuing representations of existing facts or circumstances. Any material or substantive change relating to the authorization must be promptly reported to BIS, whether status has been granted or is still under consideration. The provisions ensure that approved IC designer status, and decision-making about whether to grant this status, is informed by the most up-to-date information.

Paragraph (b) requires the requester retain records relating to all requests submitted pursuant to § 748.16 in accordance with the recordkeeping requirements set forth in part 762 of the EAR. This is to ensure that in the event of an investigation, BIS can request access to relevant facts and representations made in the course of attaining and maintaining list status.

Paragraph (c) identifies the information that authorized IC designers are required to report to the ''front-end fabricators'' producing their ICs classified under ECCN 3A090.a, which the ''front-end fabricators'' must then report to BIS. These reporting requirements are in § 743.9 Reporting Requirements for authorized IC designers, which was discussed in section III.C.

Finally, entities listed as approved IC designers and approved ''OSAT'' companies may request their removal of their listing in supplement nos. 6 or 7 to part 740 of the EAR by following the instructions in paragraph (a)(2) of this section. Paragraph (d) notes that recordkeeping and reporting to the ''front-end fabricator'' or ''front-end fabricators'' must continue until the EAR has been updated to remove the entity from supplement nos. 6 or 7 to part 740 of the EAR. Any End-user Review Committee member has authority to make a proposal for an addition to, modification of, or removal of an entry from the IC Designer list and OSAT list, consistent with the authorities in supplement no. 9 to part 748 of the EAR.

E. New Definitions

Section 772.1 is amended by adding five definitions: ''16/14 nanometer node,'' ''Aggregated approximated transistor count,'' ''Applicable advanced logic integrated circuits,'' ''Front-end fabricator,'' and ''Outsourced Semiconductor Assembly and Test (OSAT).'' These terms are added to § 772.1 to assist the public to easily find the definition for these terms, because they are used in multiple parts of the EAR. The new definitions for ''16/14 nanometer node,'' ''Aggregated approximated transistor count,'' and ''Applicable advanced logic integrated circuits'' defines these technical terms in a way that will add greater specificity under the EAR for where these terms are used. The new definitions for ''Front-end fabricator,'' and ''Outsourced Semiconductor Assembly and Test (OSAT)'' defined these types of entities for purposes of the EAR and will make it easier for exporters, reexporters, and transferors to identify these types of entities.

This IFR also revises the definition for ''Advanced-node integrated circuits'' by amending paragraph (3) for Dynamic Random-Access Memory (DRAM) ICs by revising the memory cell area from ''less than 0.0019 μm^2'' to read ''less than 0.0026 μm^2'' and revising the memory density from ''greater than 0.288 gigabits per square millimeter'' to read ''greater than 0.20 gigabits per square millimeter.'' In addition, this rule adds the parameter of ''more than 3000 through-silicon vias per die'' to ensure that all of the DRAM ICs that are intended to be captured under this definition are caught. In addition, the word ''gigabytes'' is changed to ''gigabits'' in Note 2 to the definition. See Section III.G.i.b. for more explanation about these revisions.

F. Revisions To Clarify the Scope of ECCN 3A090.a

BIS seeks to further ensure that customers of ''front-end fabricators'' and ''OSAT'' companies, including potential shell companies, cannot evade controls on advanced computing ICs by misrepresenting the performance capabilities of their IC designs. Thus, BIS has determined that it is not sufficient for ''front-end fabricators'' to confirm the ECCN by solely relying on the attestation of the end user or other party to the transaction. Accordingly, this IFR amends supplement no. 1 to part 774 by revising ECCN 3A090.a. This IFR adds Note 1 to ECCN 3A090.a to clarify that when a ''front-end fabricator'' or ''OSAT'' company is seeking to export, reexport, or transfer (in-country) any ''applicable advanced logic integrated circuit,'' there is a presumption that the item is 3A090.a and designed or marketed for datacenter. Unless this presumption is overcome, then the ''front-end fabricator'' or ''OSAT'' company must comply with all requirements applicable to items specified in 3A090.a. The presumption can be overcome in one of following three ways:

i. If the designer of the ''applicable advanced logic integrated circuit'' is an approved or authorized IC designer.

As discussed above, approved IC designers have been vetted by the U.S. government, while, prior to April 13, 2026, authorized IC designers include all IC designers (a) headquartered in Taiwan or a destination specified in Country Group A:1 or A:5, that are neither located in nor have an ultimate parent headquartered in Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR and (b) for whom transactions are subject to the reporting requirements in § 743.9 of the EAR. After April 13, 2026, a company will be considered an authorized IC designer for a period of 180 days if it both meets those criteria and submits an application to become an approved IC designer. Structuring the ECCN in this manner allows most IC designers—as the above destinations comprise the vast majority of ''front-end fabricators''' revenues—to proceed with transactions without a license but enhances the U.S. government's visibility into this approved supply chain process. In particular, authorized IC designers headquartered in Taiwan or a destination specified in Country Group A:1 or A:5 may overcome the presumption if their ''front-end fabricators'' comply with reporting requirements for such customers. After April 13, 2026, the main way to be exempted is to become an approved IC designer (other than the 180-day route described here).

ii. If the IC die is packaged by the ''front-end fabricator'' at a location outside of Macau or a destination specified in Country Group D:5 in supplement no. 1 to part 740, then the attestation of the ''front-end fabricator'' that (a) the ''aggregated approximated transistor count'' of the final packaged IC is below 30 billion transistors, or (b) the final packaged IC does not contain high bandwidth memory (HBM) and that the ''aggregated approximated transistor count'' of the final packaged IC is below (i) 35 billion transistors for any exports, reexports, or transfers (in-country) completed in 2027; or (ii) 40 billion transistors for any exports, reexports, or transfers (in-country) completed in 2029 or thereafter, then this overcomes the presumption that the IC is specified in ECCN 3A090.a.

Packaging that is completed by the ''front-end fabricator'' itself at a location outside D:5 or Macau will enable that chipmaker to produce a credible, reliable assessment of the technical parameters of the chip. The ''front-end fabricators'' will know definitively whether the final, packaged item exceeds the applicable transistor threshold specified above if it conducts the packaging itself, and so the front-end fabricator will not need to rely solely on the customer's information.

iii. If the IC is packaged by an approved ''OSAT'' company listed in supplement no. 7 to part 740 of the EAR, then the attestation of the approved ''OSAT'' company that (a) the ''aggregated approximated transistor count'' of the final packaged IC is below 30 billion transistors, or (b) the final packaged IC does not contain high bandwidth memory (HBM) and that the ''aggregated approximated transistor count'' of the final packaged IC is below (i) 35 billion transistors for any exports, reexports, or transfers (in-country) completed in 2027; or (ii) 40 billion transistors for any exports, reexports, or transfers (in-country) completed in 2029 or thereafter, then this overcomes the presumption that the IC is specified in ECCN 3A090.a.

Because of their enhanced credibility, completion of the packaging by an approved ''OSAT'' company should produce a reliable assessment for the final item's technical specifications, given that the U.S. government has assessed those entities to accurately report the ultimate performance of a final, packaged item. If an approved ''OSAT'' company can confirm that a final item does not contain more than the applicable number of transistors (as specified based on the year of the export, reexport, or in-country transfer), then it is very unlikely such item is an advanced AI IC. Any of these three conditions would suffice to enhance the credibility of a customer's attestation as to on an IC's performance, thus enabling a potential customer to proceed without applying for a license. In the absence of an attestation of the 'total processing performance' and the 'performance density' by an approved IC designer listed in supplement no. 6 to part 740 of the EAR, any logic IC produced using the ''16/14 nanometer node'' or below, or using a non-planar transistor architecture and destined for an item with an ''aggregated approximated transistor count'' exceeding the applicable number of transistors (as specified for the year of the export, reexport, or in-country transfer) within the package, or where the ''aggregated approximated transistor count'' of the final, packaged item cannot be confirmed by the ''front-end fabricator'' or ''OSAT'' company as described above, is presumed to be a 3A090.a item designed or marketed for a datacenter.

Similarly, processing by an approved ''OSAT'' company, having been vetted by BIS and relevant interagency partners, overcomes the presumption that an ''applicable advanced logic IC'' is a 3A090.a item and designed or marketed for a datacenter.

Importantly, the presumption in ECCN 3A090 does not apply to the extent an item is classified under ECCNs 4A003.z, 4A004.z, 4A005.z, or 4A090. As a result, the changes set forth under this IFR are primarily limited to circumstances in which a ''front-end fabricator'' seeks to export an IC to a chip designer or ''OSAT'' company.

Note 2 to 3A090.a provides a definition 'approximated transistor count' of a die, which is the 'transistor density' of the die multiplied by the area of the die measured in square millimeters. The 'transistor density' of the die is the number of transistors that can be fabricated per square millimeter for the process node used to manufacture the die.

G. Amendments to the Changes Made in the FDP IFR

i. Non-Commerce Control List (CCL) Amendments.

a. Revisions to § 744.11.

This rule amends § 744.11(a)(2)(v) to harmonize the product scope of the license requirements for exports from abroad or reexports from all countries by an entity headquartered in, or whose ultimate parent is headquartered in, Macau or a destination specified in Country Group D:5 with the product scope of the license requirements in § 744.11(a)(3)(i) by an entity that is headquartered or whose ultimate parent company is headquartered in a country not specified in supplement no. 4 to part 742. Specifically, this rule adds additional ECCNs to the scope of paragraph (a)(2)(v)(A)(1), which was ECCN 3B993, and with this IFR is now ECCNs 3B001 (except 3B001.a.4, c, d, f.1, f.5, f.6, g, h, k to n, p.2, p.4, or r), 3B002 (except 3B002.c), 3B611, 3B903, 3B991 (except 3B991.b.2.a through 3B991.b.2.b), 3B992, 3B993, or 3B994.

b. Revisions to the definition of DRAM ''advanced-node integrated circuit.''

This rule updates the definition of ''advanced-node integrated circuit'' in § 772.1 for DRAM ICs to clarify that (1) the relevant cell area BIS intended to capture with its prior 18 nanometer (nm) half-pitch standard is 0.0026 square micrometers (μm^2); (2) the relevant memory density BIS intended to capture with its 18 nm half-pitch standard is 0.20 gigabits per square millimeter (Gb/mm^2); and (3) the relevant number of through-silicon vias per die intended to be captured is a parameter of ''more than 3000 through-silicon vias per die''. In October 2022, BIS defined advanced-node DRAM ICs for purposes of §§ 744.6(c)(2) and 744.23(a)(2) as those with an ''18 nm

half pitch or below.'' Based on the parameters specified for ''18 nm half-pitch'' DRAM in the International Roadmap for Devices and Systems (IRDS), this standard corresponds to a DRAM cell size of 0.00194 μm^2 and a memory density of 0.288 Gb/mm^2. In the FDP IFR, BIS replaced the 18 nm half-pitch standard by directly referencing these technical parameters.

However, based on further analysis of DRAM production information, BIS determined that the IRDS definition of ''18 nm half-pitch'' does not fully cover DRAM ICs equivalent to ''18 nm half-pitch'' due to the IRDS definition and actual parameters of DRAM produced by the relevant foundries. As such, it does not restrict exports, reexports and transfers (in-country) of items covered by § 744.23(a)(2) and the activities of U.S. persons § 744.6 (c)(2)(i) to high bandwidth memory and other advanced DRAM applications. Accordingly, this update revises the cell area and memory density parameters to be consistent with production standards in the DRAM industry for the 18 nm half-pitch node, rather than the IRDS definition of ''18 nm half-pitch,'' which is based on a theoretical model, rather than actual, physical characteristics of DRAM memory. This revision imposes end use and U.S. persons controls at DRAM facilities not previously controlled by the definition of DRAM in the December 5, 2024 FDP IFR.

c. Revisions to Footnote 5-related references to address support for the ''production'' of logic and DRAM ''advanced-node integrated circuits.''

This rule expands the scope of end users covered by the new *De Minimis* and FDPs applicable to Footnote 5 entities to include any end-user facility where the ''production'' of logic and DRAM ''advanced-node integrated circuits'' occurs. As explained in the FDP IFR, BIS added 16 entities to the Entity List with a Footnote 5 designation because of specific national security and or foreign policy concerns described in the Entity List rule, including supporting, or having the potential to support, the PRC's efforts to produce ''advanced-node integrated circuits,'' including for military end uses. These controls complement BIS's existing controls on the ''production'' of ''advanced-node integrated circuits'' in §§ 744.6(c)(2) and 744.23(a)(2) of the EAR. The revisions in this IFR will ensure that controls apply to certain foreign produced items when there is ''knowledge'' that an item is destined for certain entities located at facilities of concern, whether or not they have already been added to the Entity List with a Footnote 5 designation. At this time, BIS has determined to add extraterritorial controls on facilities where the ''production'' of logic and DRAM ''advanced-node integrated circuits'' occurs.

d. Revisions to § 734.4(a)(3) text and footnote.

This rule revises the term ''a'' to ''this'' in § 734.4(a)(3) to clarify that the relevant ''commodity'' for purposes of this section is equipment described in ECCN 3B993.f.1. This IFR also updates the Footnote 1 to § 734.4 to address questions from industry about which countries maintain controls on these items.

e. Revisions to § 734.9(a) to add is-informed authority.

This rule revises § 734.9(a) by adding paragraph (a)(3) to clarify BIS's authority to notify persons that foreign-produced items located outside the United States are subject to the EAR when they meet the requirements of any FDP rule in § 734.9, which as of the effective date of this IFR consists of paragraphs (b) through (k), as well as notifying persons of any license requirements that apply to such items.

f. Correcting four note designations in § 734.9 to place them in sequential order.

In § 734.9 this IFR also redesignates four of the existing notes to place the notes in numerical order in the section for consistency with Office of Federal Register requirements for the sequential numbering of notes in a section. This IFR redesignates Note 3 to paragraph (g) as Note 4 to paragraph (g), Note 5 to paragraph (h)(2)(ii) as Note 6 to paragraph (h)(2)(ii), Note 3 to paragraph (k)(1)(ii)(B) as Note 6 to paragraph (k)(1)(ii)(B), and Note 7 to paragraph (l)(1) as Note 8 to paragraph (l)(1).

g. Addition of Note 4 to § 734.9(h)(1).

In the advanced computing FDP rule, this IFR adds Note 4 to § 734.9(h)(1) to alert fabrication facilities and ''OSAT'' companies that pursuant to Note 1 of ECCN 3A090 there is a presumption that the commodity is ECCN 3A090.a and designed or marketed for datacenters when the IC is an ''applicable advanced logic integrated circuit,'' *i.e.,* logic integrated circuits produced using the ''16/14 nanometer node'' or below, or using a non-planar transistor architecture.

h. Revision of product scope for Temporary General License (TGL)—Less restricted SME ''parts,'' ''components,'' or ''equipment.''

In supplement no. 1 to part 736, this IFR revises the product scope under paragraph (d)(1)(i)(A) for the *TGL—Less restricted SME ''parts,'' ''components,'' or ''equipment''* under paragraph (d)(1). This IFR removes the reference to ECCN 3A991 in paragraph (d)(1)(i)(A) and adds in its place 3B991 to correct the product scope.

ii. Commerce Control List Revisions.

a. Revision to add items for improving 3B001.f and 3B993.f lithography equipment.

This rule adds new paragraphs under 3B001.f, 3B993.f, 3D992, 3D993, 3E992, and 3E993 for commodities, ''software,'' and ''technology'' designed or modified to improve the minimum resolvable feature size and 'dedicated chuck overlay' of deep-ultraviolet lithography equipment specified in 3B001.f.1 and 3B993.f. These new controls cover items that would not otherwise be specified under 3B001.f.1 or 3B993.f as ''specially designed'' ''components'' or ''accessories'' for such equipment, or under related 3D and 3B ECCNs for ''software'' and ''technology'' ''specially designed'' for the ''development'' or ''production'' of such equipment.

This rule also amends various cross references in the EAR to include 3B001.f.6.

b. Revisions to ECCNs 3B993 and 3B994.

This rule amends the headings for ECCNs 3B993 and 3B994 to specify both equipment and ''specially designed'' ''components'' and ''accessories'' for commodities specified in these ECCNs. BIS is making these changes to harmonize the scope of ECCNs 3B993 and 3B994 with similar controls in ECCN 3B001 and 3B002.

c. Revisions to ECCNs 3D992, 3D993, 3D994, 3E992, 3E993, and 3E994.

Paragraphs 3D992.a, 3D993.a, 3E993.a are amended by adding ''specially designed'' for consistency with other 990 series software controls.

ECCNs 3D994 and 3E994 are amended by adding ''specially designed'' to the heading for consistency with other 990 series software and technology controls.

ECCN 3E992 is amended by adding ''and ''technology'' as follows (see List of Items Controlled)'' to the heading and adding paragraphs 3E992.a to control ''technology'' ''specially designed'' for the ''development'' or ''production'' of commodities specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r; or 3B002.c; and adding 3E992.b to control ''technology'' not specified by 3E992.a designed or modified to perform specified actions in or with deep-ultraviolet immersion photolithography equipment.

iii. Extension of comment period for FDP IFR.

This IFR extends the FDP IFR deadline for written comments to March 14, 2025. This extension is being made to allow for commenters to have additional time to review the additional

amendments and clarifications to the EAR made in the FDP IFR and to be informed by the public outreach that BIS is conducting on the FDP IFR and will be conducting for this IFR in preparing their comments. Extending the public comment period on the FDP IFR does not change that rule's effective date.

IV. Public Comments

BIS welcomes comments from the public on these additional due diligence revisions to the regulations, as well as for any of the other changes included in this IFR.

V. Savings Clauses

A. Savings Clause for the Entire IFR0

For shipments of items removed from eligibility for a license exception or export, reexport, or transfer (in-country) NLR as a result of this regulatory action that were en route aboard a carrier to a port of export, reexport, or transfer (in-country), on January 31, 2025, pursuant to actual orders for export, reexport, or transfer (in-country) to or within a foreign destination, may proceed to that destination under the previous eligibility for a License Exception or export, reexport, or transfer (in-country) NLR, provided the export, reexport, or transfer (in-country) is completed no later than on until March 3, 2025.

C. Savings Clause for This IFR for Certain Transactions Previously Authorized

If, in the twelve months prior to the effective date of this regulatory action, BIS exempted exports, reexports, or transfers (in-country) of an item from a licensing requirement imposed by notice issued pursuant to §§ 744.11(c) or 744.23(b), then exports, reexports, or transfers (in-country) of that item are exempt from any licensing requirement imposed by this regulatory action absent additional action taken by BIS.

VI. Export Control Reform Act of 2018

On August 13, 2018, the President signed into law the John S. McCain National Defense Authorization Act for Fiscal Year 2019, which included ECRA (codified, as amended, at 50 U.S.C. 4801–4852). ECRA provides the legal basis for BIS's principal authorities and serves as the authority under which BIS issues this rule. In particular, and as noted elsewhere, Section 1753 of ECRA (50 U.S.C. 4812) authorizes the regulation of exports, reexports, and transfers (in-country) of items subject to U.S. jurisdiction. Further, Section 1754(a)(1)–(16) of ECRA (50 U.S.C. 4813(a)(1)–(16)) authorizes, *inter alia,* the establishment of a list of controlled items; the prohibition of unauthorized exports, reexports, and transfers (in-country); the requirement of licenses or other authorizations for exports, reexports, and transfers (in-country) of controlled items; apprising the public of changes in policy, regulations, and procedures; and any other action necessary to carry out ECRA that is not otherwise prohibited by law. Pursuant to Section 1762(a) of ECRA (50 U.S.C. 4821(a)), these changes can be imposed in a final rule without prior notice and comment.

VII. Rulemaking Requirements

1. Executive Orders 12866, 13563, and 14094 direct agencies to assess all costs and benefits of available regulatory alternatives and, if regulation is necessary, to select regulatory approaches that maximize net benefits (including potential economic, environmental, public health and safety effects and distributive impacts and equity). Executive Order 13563 emphasizes the importance of quantifying both costs and benefits and of reducing costs, harmonizing rules, and promoting flexibility. Pursuant to Executive Order 12866, as amended, this final rule has not been determined to be a ''significant regulatory action.''

2. Notwithstanding any other provision of law, no person is required to respond to, nor shall any person be subject to a penalty for failure to comply with, a collection of information subject to the requirements of the Paperwork Reduction Act of 1995 (PRA) (44 U.S.C. 3501 *et seq.*), unless that collection of information displays a currently valid Office of Management and Budget (OMB) Control Number.

This rule involves the following OMB-approved collections of information subject to the PRA:

- 0694–0088, ''Multi-Purpose Application,'' which carries a burden hour estimate of 29.4 minutes for a manual or electronic submission;
- 0694–0096 ''Five Year Records Retention Period,'' which carries a burden hour estimate of less than 1 minute;
- 0694–0122, ''Licensing Responsibilities and Enforcement;'' which carries a burden hour estimate of 10 minutes per electronic submission;
- 0694–0137, ''License Exceptions and Exclusions;'' which carries a burden hour estimate of 5 minutes per electronic submission; and
- 0607–0152 ''Automated Export System (AES) Program,'' which carries a burden hour estimate of 3 minutes per electronic submission.

This IFR will affect the collection under control number 0694–0088, for the multipurpose application because of the increase of 375 more license applications. BIS estimates that the changes included in this IFR will result in a net increase of 375 multi-purpose applications (*i.e.,* an increase of 375 license applications) submitted annually to BIS. However, the increase in burden falls within the existing burden estimates currently associated with these control numbers.

This IFR also involves a collection previously approved by the OMB under control number 0694–0137, ''License Exceptions and Exclusions'' because this rule modifies two EAR license exceptions, which now include new notification and reporting requirements. Specifically, this IFR adds two new types of requests that can be made under the existing advisory opinion process and new reporting requirements. There are two types of entities specified in Note 1 to 3A090.a that require submissions of requests to be added, modified or removed as an approved IC designer or approved ''OSAT'' company. These new reporting requirements related to License Exceptions ACM and AIA are specified under §§ 743.9 and new Note 1 to 3A090.a of the EAR. These changes are expected to result in an increase of 1,704 submissions related to this use of License Exceptions AIA and ACM, submitted to BIS or to other parties involved in the transaction. BIS estimates that these changes will result in an increase in burden hours of 385 hours. This collection of information fits within the scope of this information collection.

Additional information regarding these collections of information—including all background materials—can be found at: *https://www.reginfo.gov/public/do/PRAMain* by using the search function to enter either the title of the collection or the OMB Control Number.

3. This rule does not contain policies with federalism implications as that term is defined in Executive Order 13132.

4. Pursuant to Section 1762 of ECRA (50 U.S.C. 4821), this action is exempt from the Administrative Procedure Act (APA) (5 U.S.C. 553) requirements for notice of proposed rulemaking, opportunity for public participation, and delay in effective date. While Section 1762 of ECRA on its own provides sufficient authority for such an exemption, this action is also independently exempt from the same APA requirements because it involves a military or foreign affairs function of the United States (5 U.S.C. 553(a)(1)). Nonetheless, BIS is accepting comments on this IFR.

5. Because a notice of proposed rulemaking and an opportunity for public comment are not required to be given for this rule under the APA (5 U.S.C. 553) or by any other law, the analytical requirements of the Regulatory Flexibility Act (5 U.S.C. 601 *et seq.*) are not applicable. Accordingly, no regulatory flexibility analysis is required, and none has been prepared.

List of Subjects

15 CFR Part 734

Administrative practice and procedure, Exports, Inventions and patents, Research, Science and technology.

15 CFR Part 740

Administrative practice and procedure, Exports, Reporting and recordkeeping requirements.

15 CFR Part 742

Exports, Terrorism.

15 CFR Part 744

Exports, Reporting and recordkeeping requirements, Terrorism.

15 CFR Part 748

Administrative practice and procedure, Exports, Reporting and recordkeeping requirements, Terrorism.

15 CFR Parts 736 and 772

Exports.

15 CFR Part 762

Administrative practice and procedure, Business and industry, Confidential business information, Exports, Reporting and recordkeeping requirements.

15 CFR Part 774

Exports, Reporting and recordkeeping requirements.

For the reasons stated in the preamble, parts 734, 736, 740, 742, 744, 748, 762, 772, and 774 of the Export Administration Regulations (15 CFR parts 730 through 774) are amended as follows:

PART 734—SCOPE OF THE EXPORT ADMINISTRATION REGULATIONS

■ 1. The authority citation for part 734 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* E.O. 12938, 59 FR 59099, 3 CFR, 1994 Comp., p. 950; E.O. 13020, 61 FR 54079, 3 CFR, 1996 Comp., p. 219; E.O. 13026, 61 FR 58767, 3 CFR, 1996 Comp., p. 228; E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783; E.O. 13637, 78 FR 16129, 3 CFR, 2014 Comp., p. 223; Notice of November 7, 2024, 89 FR 88867 (November 8, 2024).

■ 2. Section 734.4 is amended by revising paragraphs (a)(3), (8), and (9) to read as follows:

§ 734.4 *De minimis* U.S. content.

(a) * * *

(3) There is no *de minimis* level for equipment meeting the parameters in ECCN 3B993.f.1 of the Commerce Control List in supplement no. 1 to part 774 of the EAR, when the equipment is destined for use in the ''development'' or ''production'' of ''advanced-node integrated circuits'' and the ''advanced-node integrated circuits'' meet the parameter specified in paragraph (1) of that definition in § 772.1 of the EAR, unless the country from which the foreign-made item was first exported [1] has this commodity specified on an export control list.

* * * * *

(8) There is no *de minimis* level related to the SME FDP rule for a commodity meeting the parameters in ECCNs 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, or 3B002.c of the Commerce Control List (CCL) in supplement no. 1 to part 774 of the EAR, when the commodity contains a U.S.-origin integrated circuit specified under Category 3, 4, or 5 of the CCL, and the commodity is destined for Macau or a destination specified in Country Group D:5, unless excluded from the national security license requirement in § 742.4(a)(4) or the regional stability license requirement in § 742.6(a)(6) of the EAR.

(9) For items related to the Footnote 5 FDP rule, there is no *de minimis* level for an item meeting the parameters in ECCNs specified in Category 3B (except 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, or 3B002.c) of the Commerce Control List (CCL) in supplement no. 1 to part 774 of the EAR, when the commodity contains a U.S.-origin integrated circuit specified under Category 3, 4, or 5 of the CCL, and the commodity is destined for an entity with a Footnote 5 designation in the license requirement column of the Entity List in supplement no. 4 to part 744 of the EAR, or to an end-user ''facility'' located in Macau or a destination specified in Country Group D:5 when there is ''knowledge'' that the commodities will be used in the ''production'' of logic or DRAM ''advanced-node integrated circuits.''

* * * * *

[1] The Government of Japan added ArF-wet lithography equipment and other advanced semiconductor manufacturing equipment to its control list for all regions on July 23, 2023. The Government of the Kingdom of the Netherlands added this equipment to its control list for all regions on September 9, 2024.

■ 3. Section 734.9 is amended by:

■ a. Revising the paragraph heading of paragraph (a) and adding paragraph (a)(3);

■ b. Revising paragraphs (e)(3) introductory text, (e)(3)(i) introductory text; and (e)(3)(ii);

■ c. Redesignating Note 3 to paragraph (g) as Note 4 to paragraph (g), Note 5 to paragraph (h)(2)(ii) as Note 6 to paragraph (h)(2)(ii), Note 3 to paragraph (k)(1)(ii)(B) as Note 7 to paragraph (k)(1)(ii)(B) and Note 7 to paragraph (l)(1) as Note 8 to paragraph (l)(1);

■ d. Adding Note 5 to paragraph (h)(1); and

■ e. Revising paragraph (k)(1) introductory text.

The additions and revisions read as follows:

§ 734.9 Foreign-Direct Product (FDP) Rules.

* * * * *

(a) Definitions, model certification, and is-informed authority—

* * * * *

(3) *Jurisdiction and license requirements for persons informed by BIS.* BIS may inform persons, either individually by specific notice or through amendment to the EAR, that foreign-produced items located outside the United States are subject to the EAR pursuant to § 734.9, and of any license requirements that apply to such items. Specific notice will be given only by, or at the direction of, the Principal Deputy Assistant Secretary for Strategic Trade and Technology Security or the Deputy Assistant Secretary for Strategic Trade. When such notice is provided orally, it will be followed by written notice within two working days signed by one of those officials or their designee. The absence of BIS notification does not excuse the exporter from compliance with other requirements of this section.

(e) * * *

(3) *Entity List FDP rule: Footnote 5 and* ''*advanced-node integrated circuit*'' ''*production.*'' A foreign-produced commodity is subject to the EAR if it meets both the product scope in paragraph (e)(3)(i) of this section and the end-user scope in paragraph (e)(3)(ii) of this section. See § 744.11(a)(2)(v) of the EAR for license requirements, exclusion from license requirements, and license review policy, applicable to foreign-produced commodities that are subject to the EAR pursuant to this paragraph (e)(3).

(i) *Product scope Entity List FDP rule: footnote 5 and* ''*advanced-node integrated Circuit*'' ''*Production.*'' The product scope applies if a foreign-

produced commodity is specified in ECCN 3B001 (except 3B001.a.4, c, d, f.1, f.5, f.6, g, h, k to n, p.2, p.4, r), 3B002 (except 3B002.c), 3B903, 3B991 (except 3B991.b.2.a through 3B991.b.2.b), 3B992, 3B993, or 3B994, and meets the conditions of either paragraph (e)(3)(i)(A) or (B) of this section.

* * * * *

(ii) *End-user scope of the Entity List FDP rule: Footnote 5 and for entities located at ''facilities'' where ''advanced-node integrated circuit'' ''production'' occurs.* A foreign-produced commodity meets the end-user scope of this paragraph (e)(3)(ii) if there is ''knowledge'' that:

(A) *Activities involving Footnote 5 designated entities and for entities located at ''facilities'' where the ''production'' of ''advanced-node integrated circuits'' occurs.* The foreign-produced commodity will be incorporated into any ''part,'' ''component,'' or ''equipment'' produced, purchased, or ordered by any entity with a Footnote 5 designation in the license requirement column of the Entity List in supplement no. 4 to part 744 of the EAR or by an entity located at a ''facility'' in Macau or a destination specified in Country Group D:5 where the ''production'' of logic or DRAM ''advanced-node integrated circuits'' occurs; *or*

(B) *Footnote 5 designated entities and for ''advanced-node integrated circuits'' ''production'' ''facilities'' as transaction parties.* Any entity with a Footnote 5 designation in the license requirement column of the Entity List in supplement no. 4 to part 744 of the EAR or an entity located at a ''facility'' located in Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 where the ''production'' of logic or DRAM ''advanced-node integrated circuits'' occurs is a party to any transaction involving the foreign-produced commodity (*e.g.,* as a ''purchaser,'' ''intermediate consignee,'' ''ultimate consignee,'' or ''end-user'').

* * * * *

(h) * * *

(1) * * *

Note 5 to paragraph (h)(1): *See Note 1 to ECCN 3A090, because when a ''front-end fabricator'' or ''OSAT'' company is seeking to export, reexport, or transfer (in-country) an ''applicable advanced logic integrated circuit,'' there is a presumption that the commodity is 3A090.a and designed or marketed for datacenters.*

* * * * *

(k) * * *

(1) *Product scope.* The product scope applies to a foreign-produced commodity specified in ECCN 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, or 3B002.c that meets the conditions of either paragraph (k)(1)(i) or (ii) of this section.

PART 736—GENERAL PROHIBITIONS

■ 4. The authority citation for part 736 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* E.O. 12938, 59 FR 59099, 3 CFR, 1994 Comp., p. 950; E.O. 13020, 61 FR 54079, 3 CFR, 1996 Comp., p. 219; E.O. 13026, 61 FR 58767, 3 CFR, 1996 Comp., p. 228; E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783; E.O. 13338, 69 FR 26751, 3 CFR, 2004 Comp., p. 168; Notice of May 8, 2024, 89 FR 40355 (May 9, 2024); Notice of November 7, 2024, 89 FR 88867 (November 8, 2024).

■ 5. Supplement no. 1 to part 736 is amended by revising paragraphs (d)(1)(i)(A) to read as follows:

Supplement No. 1 to Part 736—General Orders

* * * * *

(d) * * *

(1) * * *

(i) * * *

(A) ECCNs that are designated as controlled on the CCL only for AT reasons (3B~~A~~991, 3B992, and associated ''software'' and ''technology''); or

* * * * *

PART 740—LICENSE EXCEPTIONS

■ 6. The authority citation for part 740 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* 22 U.S.C. 7201 *et seq.;* E.O. 13026, 61 FR 58767, 3 CFR, 1996 Comp., p. 228; E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783.

■ 7. Section 740.2 is amended by revising paragraph (a)(9)(i) to read as follows:

§ 740.2 Restrictions on all License Exceptions.

(a) * * *

(9) * * *

(i) The item is controlled under ECCN 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, 3B002.c, 3B993, 3B994, or associated software and technology in ECCN 3D001, 3D002, 3D003, 3D992, 3D993, 3D994, 3E001, 3E992, 3E993, or 3E994 and is being exported, exported from abroad, reexported, or transferred (in-country) to or within either Macau or a destination specified in Country Group D:5 of supplement no. 1 to this part, and the license exception is other than License Exception GOV, restricted to eligibility under the provisions of § 740.11(b).

* * * * *

■ 8. Section 740.26 is amended by revising paragraph (c)(1) to read as follows:

§ 740.26 License Exception Restricted Fabrication ''Facility'' (RFF)

* * * * *

(c) * * *

(1) Items may not be used for the operation, installation, maintenance, repair, overhaul, or refurbishing of items specified in ECCNs 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, 3B002.c, 3B993, or 3B994 at a 'restricted fabrication facility'.

* * * * *

■ 9. Section 740.27 is amended by revising paragraph (a)(1) to read as follows:

§ 740.27 License Exception Artificial Intelligence Authorization (AIA).

(a) * * *

(1) Eligible commodities for this exception are those specified in ECCNs 3A001.z.1.a, z.2.a, z.3.a, z.4.a; 3A090.a, if designed by an approved or authorized integrated circuit designer, as described in Note 1 to ECCN 3A090.a; 4A003.z.1.a, z.2.a; 4A004.z.1; 4A005.z.1; 4A090.a; 5A002.z.1.a, z.2.a, z.3.a, z.4.a, z.5.a, if designed by an approved or authorized integrated circuit designer, as described in Note 1 to ECCN 3A090.a; 5A004.z.1.a, z.2.a; and 5A992.z.1, if designed by an approved or authorized integrated circuit designer, as described in Note 1 to ECCN 3A090.a.

* * * * *

■ 10. Section 740.28 is amended by revising paragraph (b) to read as follows:

§ 740.28 License Exception Advanced Compute Manufacturing (ACM).

* * * * *

(b) *Eligible commodities, software, and technology.* Commodities, ''software,'' and ''technology'' eligible for License Exception ACM are as follows: Items specified by ECCNs 3A001.z; 3A090.a. if designed by an approved or authorized integrated circuit designer, as described in Note 1 to ECCN 3A090.a; 3A090.b and c; 3D001 (for ''software'' for commodities controlled by 3A001.z or 3A090); 3E001 (for ''technology'' for commodities controlled by 3A001.z or 3A090); 4A003.z; 4A004.z; 4A005.z; 4A090; 4D001 (for ''software'' for commodities controlled by 4A003.z, 4A004.z, and 4A005.z); 4D090 (for ''software'' for commodities controlled by 4A090); 4E001 (for commodities controlled by 4A003.z, 4A004.z, 4A005.z, 4A090 or ''software'' specified by 4D001 (for 4A003.z, 4A004.z, or 4A005.z), or 4D090 (for ''software'' for commodities controlled by 4A090)); 5A002.z.1.a,

z.2.a, z.3.a, z.4.a, z.5.a, if designed by an approved or authorized integrated circuit designer, as described in Note 1 to ECCN 3A090.a; 5A002.z.2; 5A004.z.2; and 5A992.z.2; 5A004.z; 5A992.z.1, if designed by an approved or authorized integrated circuit designer, as described in Note 1 to ECCN 3A090.a 5A992.z.2; 5D002.z; 5D992.z; 5E002 (for ''technology'' for commodities controlled by 5A002.z or 5A004.z or ''software'' specified by 5D002 (for 5A002.z or 5A004.z commodities)); or 5E992 (for ''technology'' for commodities controlled by 5A992.z or ''software'' controlled by 5D992.z).

* * * * *

■ 11. Supplements no. 6 and 7 are added to read as follows:

Supplement No. 6 to Part 740—Approved Integrated Circuit Designers

Note: *See Note 1 to ECCN 3A090.a.*

Advanced Micro Devices, Inc.;
Alphabet, Inc.;
Amazon.com, Inc.;
Analog Devices, Inc.;
Apple, Inc.;
BAE Systems, Inc.;
Block, Inc.;
The Boeing Company;
Broadcom, Inc.;
Cerebras Systems, Inc.;
Cisco Systems, Inc.;
Hewlett Packard Enterprise Company;
Honeywell International, Inc.;
Infineon Technologies AG;
Intel Corporation;
International Business Machines Corporation (IBM);
L3Harris Technologies, Inc.;
Marvell Technology, Inc.;
MediaTek, Inc.;
Meta Platforms, Inc.;
Micron Technology, Inc.;
Microsoft Corporation;
Mitsubishi Group;
Nokia Corporation;
Nvidia Corporation;
NXP Semiconductors NV;
Qualcomm, Inc.;
Raytheon Company;
Realtek Semiconductor Corporation;
Sony Group Corporation;
Tesla, Inc.;
Texas Instruments; *and*
Western Digital Technologies, Inc.

Supplement No. 7 to Part 740—Approved ''OSAT'' Companies

Note: *See Note 1 to ECCN 3A090.a.*

Amkor Technology, Inc.;
Ardentec Corporation;
ASE Technology Holding Co., Ltd.;
Doosan Tesna, Inc.;
Fabrinet;
Giga Solution Tech. Co., Ltd.;
GlobalFoundries, Inc.
HT Micron Semicondutores SA;
Intel Corporation;
International Business Machines Corporation (IBM);
KESM Industries Berhad;
LB Semicon, Inc.;
Micro Silicon Electronics Co., Ltd.;
Nepes Corporation;
Powertech Technology, Inc. (PTI);
QP Technologies;
Raytek Semiconductor, Inc.;
Samsung Electronics Co. Ltd.;
SFA Semicon Co., Ltd.;
Shinko Electric Industries Co. Ltd.;
Sigurd Microelectronics Corporation;
Steco Co., Ltd.;
Taiwan Semiconductor Manufacturing Company Limited (TSMC); *and*
United Microelectronics Corporation (UMC).

PART 742—CONTROL POLICY—CCL BASED CONTROLS

■ 12. The authority citation for part 742 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* 22 U.S.C. 3201 *et seq.;* 42 U.S.C. 2139a; 22 U.S.C. 7201 *et seq.;* 22 U.S.C. 7210; Sec. 1503, Pub. L. 108–11, 117 Stat. 559; E.O. 12058, 43 FR 20947, 3 CFR, 1978 Comp., p. 179; E.O. 12851, 58 FR 33181, 3 CFR, 1993 Comp., p. 608; E.O. 12938, 59 FR 59099, 3 CFR, 1994 Comp., p. 950; E.O. 13026, 61 FR 58767, 3 CFR, 1996 Comp., p. 228; E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783; Presidential Determination 2003–23, 68 FR 26459, 3 CFR, 2004 Comp., p. 320; Notice of November 1, 2023, 88 FR 75475 (November 3, 2023).

■ 13. Section 742.4 is amended by revising paragraph (a)(4)(i) to read as follows:

§ 742.4 National Security.

(a) * * *

(4) * * *

(i) *Scope.* A license is required for exports, reexports, exports from abroad, and transfers (in-country) to or within either Macau or a destination specified in Country Group D:5 in supplement no. 1 to part 740 of the EAR of items specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, 3B002.c, 3D992, or 3E992.

* * * * *

■ 14. Section 742.6 is amended by revising paragraph (a)(6)(i)(A)(*1*) to read as follows:

§ 742.6 Regional Stability.

(a) * * *

(6) * * *

(i) * * *

(A) * * *

(*1*) *Scope.* A license is required for exports, reexports, and transfers (in-country) to or within either Macau or a destination specified in Country Group D:5 in supplement no. 1 to part 740 of the EAR of items specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, 3B002.c, 3D992, or 3E992.

* * * * *

PART 743—SPECIAL REPORTING AND NOTIFICATION

■ 15. The authority citation for part 743 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783; E.O. 13637, 78 FR 16129, 3 CFR, 2014 Comp., p. 223; 78 FR 16129.

■ 16. Section 743.9 is added to read as follows:

§ 743.9 Reporting requirements for ''front-end fabricators'' producing ''applicable advanced logic integrated circuits'' for authorized integrated circuit designers.

(a) *Requirement.* ''Front-end fabricators'' producing any integrated circuit specified under ECCN 3A090.a or presumed to be specified under ECCN 3A090.a by Note 1 to 3A090 for any authorized integrated circuit designer must submit reports to BIS in accordance with this section. Reports need not, however, include information about exports, reexports, or in-country transfers to an entity that is both an approved integrated circuit designer listed in supplement no. 6 to part 740 of the EAR and an authorized integrated circuit designer, as described in Note 1 to ECCN 3A090.a.

(b) *Information to be included in the reports.* The following information must be collected by the ''front-end fabricator'' and included in each report to BIS:

(1) The name, address, and point of contact of the authorized integrated circuit designer;

(2) The ''front-end fabricator's'' name and address must appear at the top of each page;

(3) The end-user Know Your Customer (KYC) vetting form included in supplement no. 2 of this part;

(4) Description of each category of integrated circuit classified under ECCN 3A090.a sold by the ''front-end fabricator'' to the authorized integrated circuit designer during the reporting quarter, including all of the following:

(i) Designer of the integrated circuit classified under ECCN 3A090.a;

(ii) Product names associated with the integrated circuit specified or presumed to be specified under ECCN 3A090.a, including model number (if known); and

(iii) Quantity of the integrated circuits classified under ECCN 3A090.a sold by the ''front-end fabricator'' to the integrated circuit designer during the reporting quarter.

(c) *Quarterly reporting requirement.* (1) You must submit the first report by May 31, 2025. The report shall cover any exports, reexports, or transfers (in-

country) of integrated circuits classified under ECCN 3A090.a during the time between January 15, 2025 and April 30, 2025. Thereafter, reports are due according to the provisions of paragraph (c)(2) of this section.

(2)(i) After May 31, 2025, you must submit a report for each reporting period. There are four reporting periods:

(A) May 1 to July 31;

(B) August 1 to October 31;

(C) November 1 to January 31; and

(D) February 1 to April 30.

(ii) The report for a given period shall cover any exports, reexports, or transfers (in-country) of integrated circuits classified under ECCN 3A090.a during that period. Each report is due no later than 30 days after the end of the relevant reporting period.

(d) *Where to submit reports required under this section.* Reports may be emailed to *EAR.Reports@bis.doc.gov* and must specify ''Authorized integrated circuit designer'' in the subject line.

(e) *Contacts.* General information or questions about these reports can be directed to the Office of National Security Controls, Tel. (202) 482–0092, or Email: *EAR.Reports@bis.doc.gov.*

■ 17. Supplement no. 2 is added to read as follows:

Supplement No. 2 to Part 743 Authorized Integrated Circuit Designer Know Your Customer (KYC) Vetting Form

This supplement contains a questionnaire that must be completed as part of the reporting requirements for authorized integrated circuit designers in § 743.9 of the EAR. The questions in the form are KYC best practices that are especially critical in this context where there is a risk of companies seeking advanced foundry services in circumvention of controls on advanced computing items. They are not an exhaustive list of due diligence requirements but provide important information that should be part of KYC screening.

VETTING FOR AUTHORIZED INTEGRATED CIRCUIT DESIGNER

	Yes/no	If yes, insert how you resolved column 2
Section 1: Legitimacy of the authorized integrated circuit designer:		
1.A. Does the entity lack a website?		
1.B. Does the entity's website IP address correspond to a different geographical region than the entity's physical address?		
1.C. Is the country code of the entity's phone number different than the entity's physical address?		
1.D. Does the entity's email address *not* contain the company domain name?		
1.E. Is the entity's physical address invalid?		
1.F. Is the entity purportedly a civil end user but its address is co-located with a military ''facility''?		
1.G. Do publicly available corporate records contradict the entity's assertions regarding its business (*e.g.,* entity claims to be a large enterprise, but filings show only a small number of employees)?		
Section 2: Screening:		
2.A. Does the entity's name match an entry in the Consolidated Screening List?		
2.B. Does the entity's address match an entry in the Consolidated Screening List?		
2.C. Does the customer's senior management or technical leadership (*e.g.,* process engineers that are team leaders or otherwise leading development or production activities) overlap with an entity on the Consolidated Screening List?		
Section 3: Additional Party Screening:		
3.A. Are any companies within the entity's corporate hierarchy (*i.e.,* parent, subsidiary, ultimate beneficial owner) headquartered in Macau or Country Group D:5 in supplement no. 1 to part 740 of the EAR?		
3.B. Do any companies within the entity's corporate hierarchy (*i.e.,* parent, subsidiary, ultimate beneficial owner) match an entry or address in the Consolidated Screening List?		
3.C. Are any other parties to the transaction (*e.g.,* parties described in § 748.5 of the EAR) located or headquartered in Macau or Country Group D:5 in supplement no. 1 to part 740 of the EAR?		
Section 4: General Red Flags:		
4.A. Is the entity's stated end use inconsistent with the nature of their business?		
4.B. Is the requested quantity inconsistent with the entity's size?		
4.C. Is a freight forwarding firm listed as the final destination?		
4.D. Does the transaction involve multiple freight forwarders located in third countries?		
4.E. Has the entity refused to answer questions about the end users and end uses of the product?		
4.F. Do supporting documents such as commercial invoices list parties that are not the entity?		
4.G. Is the entity overpaying for a product based on known market prices?		
4.H Does the transaction involve payments from entities in third countries not otherwise involved in the transaction?		

PART 744—CONTROL POLICY: END-USER AND END-USE BASED

■ 18. The authority citation for part 744 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* 22 U.S.C. 3201 *et seq.;* 42 U.S.C. 2139a; 22 U.S.C. 7201 *et seq.;* 22 U.S.C. 7210; E.O. 12058, 43 FR 20947, 3 CFR, 1978 Comp., p. 179; E.O. 12851, 58 FR 33181, 3 CFR, 1993 Comp., p. 608; E.O. 12938, 59 FR 59099, 3 CFR, 1994 Comp., p. 950; E.O. 13026, 61 FR 58767, 3 CFR, 1996 Comp., p. 228; E.O. 13099, 63 FR 45167, 3 CFR, 1998 Comp., p. 208; E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783; E.O. 13224, 66 FR 49079, 3 CFR, 2001 Comp., p. 786; Notice of September 18, 2024, 89 FR 77011 (September 20, 2024); Notice of November 7, 2024, 89 FR 88867 (November 8, 2024).

■ 19. Section 744.6 is amended by revising paragraph (c)(2)(iii) to read as follows:

§ 744.6 Restrictions on specific activities of ''U.S. Persons.''

* * * * *

(c) * * *

(2) * * *

(iii) *Semiconductor manufacturing equipment.* To or within either Macau or a destination specified in Country Group D:5, any item not subject to the EAR and meeting the parameters of ECCNs 3B001.a.4, c, d, f.1, f.5, f.6, k to

n, p.2, p.4, r, 3B002.c, 3D992, or 3E992 regardless of end use or end user.

* * * * *

■ 20. Section 744.11 is amended by revising paragraph (a)(2)(v) paragraph heading, paragraphs (a)(2)(v)(A) introductory text, and (a)(2)(v)(A)(1), to read as follows:

§ 744.11 License requirements that apply to entities acting or at significant risk of acting contrary to the national security or foreign policy interests of the United States.

* * * * *

(a) * * *

(2) * * *

(v) *Footnote 5 entities and end-user facilities where the ''production'' of logic or DRAM ''advanced-node integrated circuits'' occurs.*

(A) *License requirement.* You may not, without a license, reexport, export from abroad, or transfer (in-country) to or within any destination or to any end user or party any foreign-produced item subject to the EAR pursuant to §§ 734.4(a)(9) or 734.9(e)(3), for each of the following paragraphs (A)(*1*) through (A)(*4*):

(*1*) *Exports from abroad or reexports from all countries.* A license is required for commodities specified in ECCNs 3B001 (except 3B001.a.4, c, d, f.1, f.5, f.6, g, h, k to n, p.2, p.4, or r), 3B002 (except 3B002.c), 3B611, 3B903, 3B991 (except 3B991.b.2.a through 3B991.b.2.b), 3B992, 3B993, or 3B994 when exported from abroad or reexported by an entity headquartered in, or whose ultimate parent company is headquartered in, Macau or a destination specified in Country Group D:5.

* * * * *

PART 748—APPLICATIONS (CLASSIFICATION, ADVISORY, AND LICENSE) AND DOCUMENTATION

■ 21. The authority citation for part 748 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* E.O. 13026, 61 FR 58767, 3 CFR, 1996 Comp., p. 228; E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783; Notice of August 13, 2024, 8 FR 66187 (August 15, 2024).

■ 22. Section 748.3 is amended by:

■ a. Redesignating paragraph (c)(4) as paragraph (c)(5); and

■ b. Adding a new paragraph (c)(4).

The addition reads as follows:

§ 748.3 Classification requests and advisory opinions.

* * * * *

(c) * * *

(4) To request an addition or modification to or removal from the approved integrated circuit designers list in supplement no. 6 to part 740 of the EAR or the approved ''OSAT'' companies list in supplement no. 7 to part 740 of the EAR, see § 748.16 of this part.

* * * * *

■ 23. Section 748.16 is added to read as follows:

§ 748.16 Approved integrated circuit designers list and approved ''OSAT'' companies list, addition, removal, or modification requests.

You must submit an advisory opinion, in accordance with § 748.3 of this part and the provisions in this section, to request an addition or modification to or removal from the approved integrated circuit designers list in supplement no. 6 to part 740 of the EAR, or the approved ''OSAT'' companies list in supplement no. 7 to part 740 of the EAR. The advisory opinion request must adhere to the provisions in paragraphs (a) through (d) of this section. Denied requests do not result in new license requirements or render the applicant ineligible for license approvals from BIS, nor does a denied request preclude a company from submitting a subsequent request.

(a)(1) *Requests to be added.* Only entities not headquartered or having an ultimate parent headquartered in Macau or a destination specified in Country Group D:5 in supplement no. 1 to part 740 will be considered for addition to either list. Only entities that have designed, assembled, tested, or packaged integrated circuits, or have credible plans to do so, will be considered for addition to either list. To ensure a thorough review, requests to be added to either list must include the information in supplement no. 4 to this part.

(2) *Requests for removal or modification.* Any listed party may request to be removed from a list or have their listing modified. If a listed entity's legal status changes (*e.g.,* is dissolved), then they must request to be removed from the appropriate list. If control of the listed entity changes or the name changes, then the company must submit a modification request. If the company can no longer abide by the provisions of the EAR that pertain to approved entities, then they must request removal from the relevant list.

(3) *Submission of requests.* All requests should be emailed to *approved_supply_chain@bis.doc.gov* with a subject line stating, ''Approved supply chain entities request.''

(4) *Review of requests for addition, modification, or removal.* The End-user Review Committee (ERC) will review all requests (additions, modifications, and removals) to both lists.

(i) The ERC will consider a range of information for requests to be added to a list, potentially including but not limited to such factors as:

(A) the applicant's record of exclusive engagement in appropriate end-use activities;

(B) the applicant's compliance with U.S. export controls;

(C) the need for an on-site review prior to approval;

(D) the applicant's capability of complying with the requirements of being added to the approved integrated circuit designers list or approved ''OSAT'' companies list;

(E) the ability of the applicant to guard against both the misuse and diversion of computing resources; and

(F) the applicant's relationships with U.S. and foreign companies. In addition, when evaluating the application, the ERC will consider the status of the export controls of the country or countries where the applicant is headquartered, and these countries' support of and adherence to multilateral export control regimes.

(ii) Requests to modify a listing due to a change in ownership or other substantive change to the listed entity will be considered in light of all of the criteria listed above. Requests to modify a listing to correct clerical errors or non-substantive changes to the listed entity's information will typically be approved.

(iii) In reviewing requests to be removed from a list, BIS will consider facts regarding the entity's compliance with the requirements of its status and the entity's rationale for removing its status. In general, requests to be removed from a list will be approved.

(5) *Approval status.* Approved integrated circuit designer and approved ''OSAT'' company status (*i.e.,* listing) is subject to revision, suspension, or revocation entirely or in part.

(6) *Continuing representations.* Information submitted in an addition or modification request is deemed to constitute continuing representations of existing facts or circumstances. Any material or substantive change relating to the request must be promptly reported to the ERC, whether approved or still under consideration.

(b) *Recordkeeping.* Records relating to all requests must be retained by the requester in accordance with the recordkeeping requirements set forth in part 762 of the EAR.

(c) *Reporting requirements.* Authorized integrated circuit designers, to be eligible for that status consistent with Note 1 to ECCN 3A090.a, are required to submit certain information

to the ''front-end fabricator,'' which the ''front-end fabricator'' must then report to BIS. See § 743.9 of the EAR.

(d) *Termination of reporting requirements.* Approved integrated circuit designers and approved ''OSAT'' companies may request to be removed from a relevant list, however, the recordkeeping requirements in paragraph (b) of this section and the reporting requirements in paragraph (c) of this section must be adhered to until the listing is removed from the relevant list.

■ 24. Supplement no. 4 is added to read as follows:

Supplement No. 4 to Part 748—Information Required To Be Submitted With a § 748.16 Request

The following information is required to be submitted with a request to be added to either supplement no. 6 to part 740—Approved Integrated Circuit Designer list or supplement no. 7 to part 740—Approved ''OSAT'' company list, as described in § 748.16. The prospective added integrated circuit designer and prospective approved ''OSAT'' company are referred to as the candidate in this supplement.

(a) *Identity.* Name of the candidate, including all names under which the candidate conducts business; complete company physical address (simply listing a post office box is insufficient); telephone number; fax number; email address; company website; and name of individual who should be contacted if BIS has any questions. If the entity submitting the request is different from the candidate identified in the request, this information must be submitted for both entities. If the candidate has multiple locations, all physical addresses must be listed.

(b) *Ownership.* Provide an overview of the structure, ownership and business of the candidate. Include a description of the entity, including type of business activity, ownership, subsidiaries, and joint-venture projects, as well as an overview of any business activity or corporate relationship that the entity has with either government or military organizations.

(c) ''*Applicable advanced logic integrated circuits.*'' List any ''applicable advanced logic integrated circuits'' the candidate expects to design, assemble, test, or package, and the end use and any known intended end uses of these commodities. Include a description of the commodities; the ECCN for all commodities, classified to the subparagraph level, as appropriate; and technical parameters for the commodities including performance specifications.

(d) *Recordkeeping.* Specify how the candidate's record keeping system will allow compliance with the recordkeeping requirements set forth in § 748.16(b) and part 762 of the EAR.

(e) *Certification.* Include an original statement on letterhead of the candidate, signed and dated by a person who has authority to legally bind the candidate, certifying that the candidate will comply with all the provisions of § 748.16.

(f) *Statement of acknowledgement and agreement.* The candidate must include this statement of acknowledgement and agreement with the request, that the candidate:

(1) Acknowledges that they have been informed of and understand that the item(s) to be produced by the ''front-end fabricator'' have been exported in accordance with the EAR and that use or diversion of such items contrary to the EAR is prohibited, particularly the license requirements of §§ 742.6(a)(6)(iii) and 744.23(a)(3) of the EAR;

(2) Agrees to comply with the recordkeeping requirements in § 748.16(b) and part 762 of the EAR; and

(3) Agrees to allow on-site reviews by U.S. Government officials to verify compliance with the EAR.

PART 762—RECORDKEEPING

■ 25. The authority citation for part 762 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783.

■ 26. Section 762.2 is amended by adding paragraphs (b)(61) and (b)(62), to read as follows:

§ 762.2 Records to be retained.

* * * * *

(b) * * *

(61) § 748.16(b), all records relating to requests for addition or modifications to or deletion from supplement no. 6 or supplement no. 7 to part 740.

(62) Supplement No. 2 to Part 743 Authorized Integrated Circuit Designer Vetting Form.

* * * * *

PART 772—DEFINITIONS OF TERMS

■ 27. The authority citation for part 772 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783.

■ 28. Section 772.1 is amended by:

■ a. Adding, in alphabetical order, the definitions for ''16/14 nanometer node;''

■ b. Revising the definition for ''Advanced-Node Integrated Circuits;''

■ c. Adding, in alphabetical order, the definitions for ''Aggregated approximated transistor count'', ''Applicable advanced logic integrated circuits'', ''Front-end fabricator'', and ''Outsourced Semiconductor Assembly and Test (OSAT)'' to read as follows:

§ 772.1 Definitions of terms as used in the Export Administration Regulations (EAR).

* * * * *

16/14 nanometer node (16/14 nm node) is indicated in the Logic Industry ''Node Range'' figure described in the International Roadmap for Devices and Systems, 2016 edition (''More Moore'' White Paper), available at: *https://irds.ieee.org/images/files/pdf/2016_MM.pdf*).

* * * * *

Advanced-Node Integrated Circuits (Advanced-Node IC). For parts 734 and 744 of the EAR, ''advanced-node integrated circuits'' include integrated circuits that meet any of the following criteria:

(1) Logic integrated circuits using a non-planar transistor architecture or with a ''production'' 'technology node' of 16/14 nanometers or less;

(2) NOT AND (NAND) memory integrated circuits with 128 layers or more; or

(3) Dynamic random-access memory (DRAM) integrated circuits having:

(i) A memory cell area of less than 0.0026 μm^2;

(ii) A memory density greater than 0.20 gigabits per square millimeter; or

(iii) More than 3000 through-silicon vias per die.

Note 1 to definition of ''Advanced-Node Integrated Circuits'': *For the purposes of paragraph (1) of this definition, the term technology node refers to the Logic Industry ''Node Range'' figure described in the International Roadmap for Devices and Systems, 2016 edition (''More Moore'' White Paper), available at: ≤https://irds.ieee.org/images/files/pdf/2016_MM.pdf.*

Note 2 to definition of ''Advanced-Node Integrated Circuits'': *For the purposes of paragraph (3) of this definition, the term memory density refers to the capacity of the monolithic die, package, or stack comprising the DRAM integrated circuit measured in gigabits divided by the relevant area. For a monolithic die, the relevant area is the area of the die. For package or stack, the relevant area is the footprint of the package or stack measured in square millimeters. In the case where a stack is contained in a package, use the area of the package. Cell area is defined as Wordline*Bitline (which takes into consideration both transistor and capacitor dimensions).*

* * * * *

Aggregated approximated transistor count means the sum of the 'approximated transistor counts,' as defined in Note 1 to 3A090.a, of each ''applicable advanced logic integrated circuit'' die within the final package fabricated using a ''16/14 nanometer node'' or below, or using a non-planar transistor architecture.

* * * * *

Applicable advanced logic integrated circuits are logic integrated circuits produced using the ''16/14 nanometer

node'' or below, or using a non-planar transistor architecture.

* * * * *

Front-end fabricator is the company that provides front-end fabrication services to produce an integrated circuit, creating circuits on the surface of a wafer through processes such as photolithography, etch, and deposition.

* * * * *

Outsourced Semiconductor Assembly and Test (OSAT) is a company that provides third-party manufacturing and testing services to semiconductor businesses. OSAT companies are responsible for assembling, packaging, and testing integrated circuits and other semiconductor devices.

* * * * *

PART 774—THE COMMERCE CONTROL LIST

■ 29. The authority citation for part 774 continues to read as follows:

Authority: 50 U.S.C. 4801–4852; 50 U.S.C. 4601 *et seq.;* 50 U.S.C. 1701 *et seq.;* 10 U.S.C. 8720; 10 U.S.C. 8730(e); 22 U.S.C. 287c, 22 U.S.C. 3201 *et seq.;* 22 U.S.C. 6004; 42 U.S.C. 2139a; 15 U.S.C. 1824; 50 U.S.C. 4305; 22 U.S.C. 7201 *et seq.;* 22 U.S.C. 7210; E.O. 13026, 61 FR 58767, 3 CFR, 1996 Comp., p. 228; E.O. 13222, 66 FR 44025, 3 CFR, 2001 Comp., p. 783.

■ 30. Supplement no. 1 to part 774 is amended by revising ECCN 3A090, 3B001, 3B993 and 3B994, 3D992, 3D993, 3D994, 3E992, 3E993, and 3E994, to read as follows:

Supplement No. 1 To Part 774—The Commerce Control List

* * * * *

3A090 Integrated circuits as follows (see List of Items Controlled).

License Requirements

Reason for Control: RS, AT

Control(s)	*Country chart (see Supp. No. 1 to part 738)*
RS applies to entire entry, except 3A090.a.	To or within any destination worldwide, see § 742.6(a)(6)(iii)(A) of the EAR.
RS applies to 3A090.b ...	To or within destinations specified in Country Groups D:1, D:4, and D:5 of supplement no. 1 to part 740 of the EAR, excluding any destination also specified in Country Groups A:5 or A:6. *See* § 742.6(a)(6)(iii)(B) of the EAR.
RS applies to 3A090.c ...	To or within Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR. See § 742.6(a)(6)(i)(B) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

LVS: N/A

GBS: N/A

NAC/ACA: Yes, for 3A090.a, if the item is not designed or marketed for use in datacenters and has a 'total processing performance' of 4800 or more; yes, for 3A090.b, if the item is designed or marketed for use in datacenters. N/A for 3A090.c.

HBM: Yes, for 3A090.c. See § 740.25 of the EAR.

AIA: Yes, for 3A090.a.

ACM: Yes

LPP: Yes for 3A090.a.

List of Items Controlled

Related Controls: (1) See ECCNs 3D001, 3E001, 5D002.z, and 5D992.z for associated technology and software controls. (2) See ECCNs 3A001.z, 5A002.z, 5A004.z, and 5A992.z.

Related Definitions: N/A

Items:

a. Integrated circuits having one or more digital processing units having either of the following:

a.1. A 'total processing performance' of 4800 or more; *or*

a.2. A 'total processing performance' of 1600 or more and a 'performance density' of 5.92 or more.

Note 1 to 3A090.a: *When a ''front-end fabricator'' or ''OSAT'' company is seeking to export, reexport, or transfer (in-country) an ''applicable advanced logic integrated circuit,'' there is a presumption that the item is 3A090.a and designed or marketed for datacenters. If the ''front-end fabricator'' or ''OSAT'' company cannot overcome this presumption, then it must comply with all license requirements applicable to items specified in 3A090.a. However, this presumption does not apply to any entity other than the ''front-end fabricator'' or ''OSAT'' company. A ''front-end fabricator'' or ''OSAT'' company can overcome this presumption in any of the following three ways outlined in paragraphs a. through c. of this Note 1.*

a. *If the designer of the ''applicable advanced logic integrated circuit'' is an approved or authorized integrated circuit designer, then a datasheet or other attestation of the 'total processing performance' and the 'performance density' from the approved or authorized integrated circuit designer indicating that the IC is not specified in 3A090.a will overcome the presumption for the ''front-end fabricator'' or ''OSAT'' company that the IC is specified in ECCN 3A090.a.*

(1) *Approved integrated circuit designers are listed in supplement no. 6 to this part of the EAR;*

(2) *Prior to April 13, 2026, authorized integrated circuit designers include all integrated circuit designers:*

(i) Headquartered in Taiwan or a destination specified in Country Group A:1 or A:5, that are neither located in nor have an ultimate parent headquartered in Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR; and

(ii) That have agreed to submit applicable information described in § 743.9(b) to the ''front-end fabricator,'' which the ''front-end fabricator'' must then report to BIS.

(3) After April 13, 2026, authorized integrated circuit designers include any integrated circuit designer that both meets the criteria specified in subparagraph (2) and has submitted an application to become an approved integrated circuit designer. However, any company deemed an authorized IC designer after April 13, 2026, will cease to be an authorized IC designer 180 days after the submission of its application to become an approved IC designer.

b. If the integrated circuit die is packaged by the ''front-end fabricator'' at a location outside of Macau or a destination specified in Country Group D:5 in supplement no. 1 to part 740, then the attestation of the ''front-end fabricator'' that (a) the ''aggregated approximated transistor count'' of the final packaged IC is below 30 billion transistors, or (b) the final packaged IC does not contain high-bandwidth memory and that the ''aggregated approximated transistor count'' of the final packaged IC is below (i) 35 billion transistors for any exports, reexports, or transfers (in-country) completed in 2027; or (ii) 40 billion transistors for any exports, reexports, or transfers (in-country) completed in 2029 or thereafter, then this overcomes the presumption by the ''front-end fabricator'' or ''OSAT'' company that the IC is specified in ECCN 3A090.a.

c. If the integrated circuit is packaged by an approved ''OSAT'' company listed in supplement no. 7 to part 740 of the EAR, then the attestation of the approved ''OSAT'' company that (a) the ''aggregated approximated transistor count'' of the final packaged IC is below 30 billion transistors, or (b) the final packaged IC does not contain high-bandwidth memory and that the ''aggregated approximated transistor count'' of the final packaged IC is below (i) 35 billion transistors for any exports, reexports, or transfers (in-country) completed in 2027; or (ii) 40 billion transistors for any exports, reexports, or transfers (in-country) completed in 2029 or thereafter, then this overcomes the presumption by the ''front-end fabricator'' or ''OSAT'' company that the IC is specified in ECCN 3A090.a.

d. It is not sufficient for the ''front-end fabricator'' or ''OSAT'' company to confirm the ECCN by relying on the attestation of the end user or other party to the transaction, except under one of the three ways enumerated in paragraphs a. through c. of this note. In the absence of an attestation of the 'total processing performance' and the 'performance density' by an approved integrated circuit designer listed in supplement no. 6 to part 740 of the EAR, the ''front-end fabricator'' or ''OSAT'' company must presume that any logic integrated circuit produced using the ''16/14 nanometer node'' or below, or using a non-planar transistor architecture and destined for a commodity with an (a) ''aggregated

approximated transistor count'' of the final packaged IC is below 30 billion transistors, or (b) the final packaged IC does not contain high-bandwidth memory and that the ''aggregated approximated transistor count'' of the final packaged IC is below (i) 35 billion transistors for any exports, reexports, or transfers (in-country) completed in 2027; or (ii) 40 billion transistors for any exports, reexports, or transfers (in-country) completed in 2029 or thereafter, or where the ''aggregated approximated transistor count,'' of the final, packaged integrated circuit cannot be confirmed by the ''front-end fabricator,'' or an approved ''OSAT'' company listed in supplement no. 7 to part 740 of the EAR, is specified in ECCN 3A090.a and designed or marketed for a datacenter.

Technical Note 1 to 3A090.a: *The 'approximated transistor count' of a die is the 'transistor density' of the die multiplied by the area of the die measured in square millimeters. The 'transistor density' of the die is the number of transistors that can be fabricated per square millimeter for the process node used to manufacture the die. To calculate the number of 'approximated transistor count' of a die, a ''front end fabricator'' or ''OSAT'' company has two options. First, the ''front end fabricator'' or ''OSAT'' company may take the transistor density of the process node used to manufacture the die and multiply this density by the area of the die. This number may be significantly higher than the true transistor count, but if the result is below the relevant transistor threshold, then the ''front end fabricator'' or ''OSAT'' company can be confident that the die in question will not exceed that threshold. Second, to adjudicate edge cases, the ''front end fabricator'' or ''OSAT'' company may use standard design verification tools to estimate the number of (both active and passive) transistors on the die using the GDS file.*

b. Integrated circuits having one or more digital processing units having either of the following:

b.1. A 'total processing performance' of 2400 or more and less than 4800 and a 'performance density' of 1.6 or more and less than 5.92, *or*

b.2. A 'total processing performance' of 1600 or more and a 'performance density' of 3.2 or more and less than 5.92.

Note 2 to 3A090.a and 3A090.b: *3A090.a and 3A090.b do not apply to items that are not designed or marketed for use in datacenters and do not have a 'total processing performance' of 4800 or more. For 3A090.a and 3A090.b items that are not designed or marketed for use in datacenters and that have a 'total processing performance' of 4800 or more, see license exceptions NAC and ACA.*

Note 3 to 3A090.a and 3A090.b: *Integrated circuits specified by 3A090 include graphical processing units (GPUs), tensor processing units (TPUs), neural processors, in-memory processors, vision processors, text processors, co-processors/accelerators, adaptive processors, field-programmable logic devices (FPLDs), and application-specific integrated circuits (ASICs). Examples of integrated circuits are in the Note to 3A001.a.*

Note 4 to 3A090.a and 3A090.b: *For integrated circuits that are excluded from ECCN 3A090 under Note 2 or 3 to 3A090, those ICs are also not applicable for classifications made under ECCNs 3A001.z, 4A003.z, 4A004.z, 4A005.z, 4A090, 5A002.z, 5A004.z, 5A992.z, 5D002.z, or 5D992.z because those other CCL classifications are based on the incorporation of an integrated circuit that meets the control parameters under ECCN 3A090 or otherwise meets or exceeds the control parameters or ECCNs 3A090 or 4A090. The performance parameters under ECCN 3A090.c are not used for determining whether an item is classified in a .z ECCN. See the Related Controls paragraphs of ECCNs 3A001.z, 4A003.z, 4A004.z, 4A005.z, 4A090, 5A002.z, 5A004.z, 5A992.z, 5D002.z, or 5D992.z.*

Technical Note 2 to 3A090.a and 3A090.b:

1. 'Total processing performance' ('TPP') is 2 × 'MacTOPS' × 'bit length of the operation', aggregated over all processing units on the integrated circuit.

a. For purposes of 3A090, 'MacTOPS' is the theoretical peak number of Tera (10^{12}) operations per second for multiply-accumulate computation ($D = A \times B + C$).

b. The 2 in the 'TPP' formula is based on industry convention of counting one multiply-accumulate computation, $D = A \times B + C$, as 2 operations for purpose of datasheets. Therefore, 2 × MacTOPS may correspond to the reported TOPS or FLOPS on a datasheet.

c. For purposes of 3A090, 'bit length of the operation' for a multiply-accumulate computation is the largest bit-length of the inputs to the multiply operation.

d. Aggregate the TPPs for each processing unit on the integrated circuit to arrive at a total. 'TPP' = TPP1 + TPP2 + ... + TPPn (where n is the number or processing units on the integrated circuit).

2. The rate of 'MacTOPS' is to be calculated at its maximum value theoretically possible. The rate of 'MacTOPS' is assumed to be the highest value the manufacturer claims in annual or brochure for the integrated circuit. For example, the 'TPP' threshold of 4800 can be met with 600 tera integer operations (or 2 × 300 'MacTOPS') at 8 bits or 300 tera FLOPS (or 2 × 150 'MacTOPS') at 16 bits. If the integrated circuit is designed for MAC computation with multiple bit lengths that achieve different 'TPP' values, the highest 'TPP' value should be evaluated against parameters in 3A090.

3. For integrated circuits specified by 3A090 that provide processing of both sparse and dense matrices, the 'TPP' values are the values for processing of dense matrices (e.g., without sparsity).

4. 'Performance density' is 'TPP' divided by 'applicable die area'. For purposes of 3A090, 'applicable die area' is measured in millimeters squared and includes all die area of logic dies manufactured with a process node that uses a non-planar transistor architecture.

c. High bandwidth memory (HBM) having a 'memory bandwidth density' greater than 2 gigabytes per second per square millimeter.

Technical Note 1 to 3A090.c: *'Memory bandwidth density' is the memory bandwidth measured in gigabytes per second divided by the area of the package or stack measured in square millimeters. In the case where a stack is contained in a package, use the memory bandwidth of the packaged device and the area of the package. High bandwidth memory (HBM) includes dynamic random access memory integrated circuits, regardless of whether they conform to the JEDEC standards for high bandwidth memory (HBM), provided they have a 'memory bandwidth density' greater than 2 gigabytes per second per square millimeter. This control does not cover co-packaged integrated circuits with both HBM and logic integrated circuit where the dominant function of the co-packaged integrated circuit is processing. It does include HBM permanently affixed to a logic integrated circuit designed as a control interface and incorporating a physical layer (PHY) function.*

* * * * *

3B001 Equipment for the manufacturing of semiconductor devices, materials, or related equipment, as follows (see List of Items Controlled) and ''specially designed'' ''components'' and ''accessories'' therefor.

License Requirements

Reason for Control: NS, RS, AT

Control(s)	*Country chart (see Supp. No. 1 to part 738)*
NS applies to 3B001.c.1.a, 3B001.c.1.c, and 3B001.q.	Worldwide control. See § 742.4(a)(5) and (b)(10) of the EAR.
RS applies to 3B001.c.1.a, 3B001.c.1.c, and 3B001.q.	Worldwide control. See § 742.6(a)(10) and (b)(11) of the EAR.
NS applies to 3B001.a.1 to a.3, b, e, f.2 to f.4, g to j.	NS Column 2.
NS applies to 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r.	To or within Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR. See § 742.4(a)(4) of the EAR.
RS applies to 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r.	To or within Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR. See § 742.6(a)(6) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

LVS: $500, except semiconductor manufacturing equipment specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r.

GBS: Yes, except a.3 (molecular beam epitaxial growth equipment using gas sources), c.1.a (Equipment designed or modified for isotropic dry etching), c.1.c (Equipment designed or modified for anisotropic dry etching), .e (automatic loading multi-chamber central wafer handling systems *only* if connected to equipment controlled by 3B001.a.3, or .f), .f (lithography equipment) and .q (''EUV'' masks and reticles designed for integrated circuits, not specified by 3B001.g, and

having a mask ''substrate blank'' specified by 3B001.j).

IEC: Yes, for 3B001.c.1.a, c.1.c, and .q, see § 740.2(a)(22) and § 740.24 of the EAR.

Special Conditions for STA

STA: License Exception STA may not be used to ship 3B001.c.1.a, c.1.c, and .q to any of the destinations listed in Country Group A:5 or A:6 (See supplement no. 1 to part 740 of the EAR).

List of Items Controlled

Related Controls: See also 3B903 and 3B991. See ECCNs 3D001, 3D992, 3E001, and 3E992 for related ''software'' and ''technology'' controls.

Related Definitions: N/A

Items:

a. Equipment designed for epitaxial growth as follows:

a.1. Equipment designed or modified to produce a layer of any material other than silicon with a thickness uniform to less than ±2.5% across a distance of 75 mm or more;

Note: *3B001.a.1 includes atomic layer epitaxy (ALE) equipment.*

a.2. Metal Organic Chemical Vapor Deposition (MOCVD) reactors designed for compound semiconductor epitaxial growth of material having two or more of the following elements: aluminum, gallium, indium, arsenic, phosphorus, antimony, oxygen, or nitrogen;

a.3. Molecular beam epitaxial growth equipment using gas or solid sources;

a.4. Equipment designed for epitaxial growth of silicon (Si) or silicon germanium (SiGe), and having all of the following:

a.4.a. At least one preclean chamber designed to provide a surface preparation means to clean the surface of the wafer; *and*

a.4.b. An epitaxial deposition chamber designed to operate at a temperature equal to or below 958 K (685 °C).

b. Semiconductor wafer fabrication equipment designed for ion implantation and having any of the following:

b.1. [Reserved]

b.2. Being designed and optimized to operate at a beam energy of 20 keV or more and a beam current of 10 mA or more for hydrogen, deuterium, or helium implant;

b.3. Direct write capability;

b.4. A beam energy of 65 keV or more and a beam current of 45 mA or more for high energy oxygen implant into a heated semiconductor material ''substrate''; *or*

b.5. Being designed and optimized to operate at beam energy of 20 keV or more and a beam current of 10mA or more for silicon implant into a semiconductor material ''substrate'' heated to 600 °C or greater;

c. Etch equipment.

c.1. Equipment designed for dry etching as follows:

c.1.a. Equipment designed or modified for isotropic dry etching, having a largest 'silicon germanium-to-silicon (SiGe:Si) etch selectivity' of greater than or equal to 100:1; *or*

c.1.b. [Reserved]

c.1.c. Equipment designed or modified for anisotropic dry etching, having all of the following;

c.1.c.1. Radio Frequency (RF) power source(s) with at least one pulsed RF output;

c.1.c.2. One or more fast gas switching valve(s) with switching time less than 300 milliseconds; *and*

c.1.c.3. Electrostatic chuck with twenty or more individually controllable variable temperature elements;

c.2. Equipment designed for wet chemical processing and having a largest 'silicon germanium-to-silicon (SiGe:Si) etch selectivity' of greater than or equal to 100:1;

c.3. Equipment designed for anisotropic dry etching having all of following:

c.3.a Two or more RF independent sources;

c.3.b Two or more independent gas sources;

c.3.c 'Process uniformity tuning' for wafer thickness variation compensation; and

c.3.d Through Silicon Via (TSV) reveal Endpoint Detection (EPD);

c.4. Equipment designed for Through Silicon Via (TSV) etch having all of the following:

c.4.a. Silicon etch rate greater than 7 microns per minute;

c.4.b. Within wafer (WIW) etch depth non-uniformity of less than or equal 2 percent; *and*

c.4.c. A Through Silicon Via (TSV) aspect ratio greater than or equal to 10:1.

Note 1: *3B001.c includes etching by 'radicals', ions, sequential reactions, or non-sequential reaction.*

Note 2: *3B001.c.1.c includes etching using RF pulse excited plasma, pulsed duty cycle excited plasma, pulsed voltage on electrodes modified plasma, cyclic injection and purging of gases combined with a plasma, plasma atomic layer etching, or plasma quasi-atomic layer etching.*

Technical Notes:

1. For the purposes of 3B001.c, 'silicon germanium-to-silicon (SiGe:Si) etch selectivity' is measured for a Ge concentration of greater than or equal to 30% ($Si_{0.70}Ge_{0.30}$).

2. For the purposes of 3B001.c Note 1 and 3B001.d.14, 'radical' is defined as an atom, molecule, or ion that has an unpaired electron in an open electron shell configuration.

3. For the purposes of 3B001.c.3, 'process uniformity tuning' is the process of compensating for incoming wafer thickness variations after grinding.

d. Semiconductor manufacturing deposition equipment, as follows:

d.1. Equipment designed for cobalt (Co) electroplating or cobalt electroless-plating deposition processes;

Note: *3B001.d.1 controls semiconductor wafer processing equipment.*

d.2. Equipment designed for:

d.2.a. Chemical vapor deposition of cobalt (Co) fill metal; or

d.2.b. Selective bottom-up chemical vapor deposition of tungsten (W) fill metal;

d.3. Semiconductor manufacturing equipment designed to fabricate a metal contact by multistep processing within a single chamber by performing all of the following:

d.3.a. Deposition of a tungsten layer, using an organometallic compound, while maintaining the wafer substrate temperature greater than 100 °C and less than 500 °C; and

d.3.b. Surface treatment plasma process using hydrogen (H2), hydrogen and nitrogen (H2+N2), or ammonia (NH3).

d.4. Equipment or systems designed for multistep processing in multiple chambers or stations, as follows:

d.4.a. Equipment designed to fabricate a metal contact by performing all of the following processes:

d.4.a.1. Surface treatment plasma process using hydrogen (H_2), including hydrogen and nitrogen ($H_2 + N_2$) or ammonia (NH_3), while maintaining the wafer substrate at a temperature greater than 100 °C and less than 500 °C;

d.4.a.2. Surface treatment plasma process using oxygen (O_2) or ozone (O_3), while maintaining the wafer substrate at a temperature greater than 40 °C and less than 500 °C; *and*

d.4.a.3. Deposition of a tungsten (W) layer while maintaining the wafer substrate temperature greater than 100 °C and less than 500 °C;

d.4.b. Equipment designed to fabricate a metal contact by performing all of the following processes:

d.4.b.1 Surface treatment process using a remote plasma generator and an ion filter; *and*

d.4.b.2. Deposition of a cobalt (Co) layer selectively onto copper (Cu) using an organometallic compound;

Note: *This control does not apply to equipment that is non-selective.*

d.4.c. Equipment designed to fabricate a metal contact by performing all the following processes:

d.4.c.1. Deposition of a titanium nitride (TiN) or tungsten carbide (WC) layer, using an organometallic compound, while maintaining the wafer substrate at a temperature greater than 20 °C and less than 500 °C;

d.4.c.2. Deposition of a cobalt (Co) layer using a physical sputter deposition technique and having a process pressure greater than 133.3 mPa and less than 13.33 Pa, while maintaining the wafer substrate at a temperature below 500 °C; *and*

d.4.c.3. Deposition of a cobalt (Co) layer using an organometallic compound and having a process pressure greater than 133.3 Pa and less than 13.33 kPa, while maintaining the wafer substrate at a temperature greater than 20 °C and less than 500 °C;

d.4.d. Equipment designed to fabricate copper (Cu) interconnects by performing all of the following processes:

d.4.d.1. Deposition of a cobalt (Co) or ruthenium (Ru) layer using an organometallic compound and having a process pressure greater than 133.3 Pa and less than 13.33 kPa, while maintaining the wafer substrate at a temperature greater than 20 °C and less than 500 °C; *and*

d.4.d.2. Deposition of a copper layer using a physical vapor deposition technique and having a process pressure greater than 133.3 mPa and less than 13.33 Pa, while maintaining the wafer substrate at a temperature below 500 °C;

d.5. Equipment designed for plasma enhanced chemical vapor deposition of carbon hard masks more than 2 um thick and with density of greater than 1.7g/cc;

d.6. Atomic Layer Deposition (ALD) equipment designed for area selective deposition of a barrier or liner using an organometallic compound;

Note: *3B001.d.6 includes equipment capable of area selective deposition of a barrier layer to enable fill metal contact to an underlying electrical conductor without a barrier layer at the fill metal via interface to an underlying electrical conductor.*

d.7. Equipment designed for Atomic Layer Deposition (ALD) of tungsten (W) to fill an entire interconnect or in a channel less than 40 nm wide, while maintaining the wafer substrate at a temperature less than 500 °C.

d.8. Equipment designed for Atomic Layer Deposition (ALD) of 'work function metal' having all of the following:

d.8.a. More than one metal source of which one is designed for an aluminum (Al) precursor;

d.8.b. Precursor vessel designed and enabled to operate at a temperature greater than 30 °C; *and*

d.8.c. Designed for depositing a 'work function metal' having all of the following:

d.8.c.1. Deposition of titanium-aluminum carbide (TiAlC); *and*

d.8.c.2. Enabling a work function greater than 4.0 eV;

Technical Note: *For the purposes of 3B001.d.8, 'work function metal' is a material that controls the threshold voltage of a transistor.*

d.9. Spatial Atomic Layer Deposition (ALD) equipment having a wafer support platform that rotates around an axis having any of the following:

d.9.a. A spatial plasma enhanced atomic layer deposition mode of operation;

d.9.b. A plasma source; *or*

d.9.c. A plasma shield or means to confine the plasma to the plasma exposure process region;

d.10. Equipment designed for Atomic Layer Deposition (ALD) or Chemical Vapor Deposition (CVD) of plasma enhanced of low fluorine tungsten (FW) (fluorine (F) concentration less than 10^{19} atoms/cm^3) films;

d.11. [Reserved]

d.12. Equipment designed for depositing a metal layer, and having any of the following:

d.12.a. Selective tungsten (W) growth without a barrier; *or*

d.12.b. Selective molybdenum (Mo) growth without a barrier;

d.13. Equipment designed for depositing a ruthenium layer (Ru) using an organometallic compound, while maintaining the wafer substrate at a temperature greater than 20 °C and less than 500 °C;

d.14. Equipment designed for deposition assisted by remotely generated 'radicals', enabling the fabrication of a silicon (Si) and carbon (C) containing film, and having all of the following properties of the deposited film:

d.14.a. A dielectric constant (k) of less than 4.4;

d.14.b. In features with an aspect ratio greater than 5:1 with lateral openings of less than 35 nm; *and*

d.14.c. A feature-to-feature pitch of less than 45 nm;

d.15. Equipment designed for void free plasma enhanced deposition of a low-k dielectric layer in gaps between metal lines less than 25 nm and having an aspect ratio greater than or equal to 1:1 with a less than 3.3 dielectric constant;

d.16. [Reserved]

d.17. Equipment designed for plasma enhanced chemical vapor deposition (PECVD) or radical assisted chemical vapor deposition and UV curing in a single platform of a dielectric film, while maintaining a substrate temperature below 500 °C, having all of the following:

d.17.a. A thickness of more than 6 nm and less than 20 nm on metal features having less than 24 nm pitch and having an aspect ratio equal to or greater than 1:1.8; *and*

d.17.b. A dielectric constant less than 3.0;

d.18. Equipment designed or modified for Atomic Layer Deposition (ALD) of molybdenum (Mo), ruthenium (Ru), or combinations Mo or Ru, and having all of the following:

d.18.a. A metal precursor source designed or modified to operate at a temperature greater 75 °C; *and*

d.18.b. A process chamber (module) using a reducing agent containing hydrogen (H) at a pressure greater than or equal to 30 Torr (4 kPa).

Note: *For the purposes of paragraph d.18.a, the metal precursor source need not be integrated with the equipment. The metal precursor could be delivered by an on-tool source or from a sub-fab source.*

d.19. Deposition equipment having direct-liquid injection of more than two metal precursors, designed or modified to deposit a conformal dielectric film with a dielectric constant (K) greater than 40 in features with aspect ratio greater than 200:1 in a single deposition chamber.

d.20. Physical vapor deposition equipment having electromagnets for ion flux guidance, and ''specially designed'' to deposit tungsten (W) metal into features having an aspect ratio of 3:1 or greater.

e. Automatic loading multi-chamber central wafer handling systems having all of the following:

e.1. Interfaces for wafer input and output, to which more than two functionally different 'semiconductor process tools' controlled by 3B001.a, .b., .c, and .d are designed to be connected; *and*

e.2. Designed to form an integrated system in a vacuum environment for 'sequential multiple wafer processing';

Note: *3B001.e does not control automatic robotic wafer handling systems ''specially designed'' for parallel wafer processing.*

Technical Notes:

1. For the purposes of 3B001.e, 'semiconductor process tools' refers to modular tools that provide physical processes for semiconductor ''production'' that are functionally different, such as deposition, implant or thermal processing.

2. For the purposes of 3B001.e, 'sequential multiple wafer processing' means the capability to process each wafer in different 'semiconductor process tools', such as by transferring each wafer from one tool to a second tool and on to a third tool with the automatic loading multi-chamber central wafer handling systems.

f. Lithography commodities as follows:

f.1. Align and expose step and repeat (direct step on wafer) or step and scan (scanner) equipment for wafer processing using photo-optical or X-ray methods and having any of the following:

f.1.a. A light source wavelength shorter than 193 nm; *or*

f.1.b. A light source wavelength equal to or longer than 193 nm and having all of the following:

f.1.b.1. The capability to produce a pattern with a ''Minimum Resolvable Feature size'' (MRF) of 45 nm or less; *and*

f.1.b.2. A maximum 'dedicated chuck overlay' value of less than or equal to 1.50 nm;

Technical Notes: *For the purposes of 3B001.f.1.b:*

1. The 'Minimum Resolvable Feature size' (MRF) (*i.e., resolution*) *is calculated by the following formula:*

$$MRF = \frac{(\text{an exposure light source wavelength in nm}) \times (K\ \text{factor})}{\text{maximum numerical aperture}}$$

where, for the purposes of 3B001.f.1.b, the K factor = 0.25 'MRF' is also known as resolution.

2. 'Dedicated chuck overlay' is the alignment accuracy of a new pattern to an existing pattern printed on a wafer by the same lithographic system. 'Dedicated chuck overlay' is also known as single machine overlay.

f.2. Imprint lithography equipment capable of production features of 45 nm or less;

Note: *3B001.f.2 includes:*

—Micro contact printing tools
—Hot embossing tools
—Nano-imprint lithography tools
—Step and flash imprint lithography (S–FIL) tools

f.3. Equipment ''specially designed'' for mask making having all of the following:

f.3.a. A deflected focused electron beam, ion beam or ''laser'' beam; *and*

f.3.b. Having any of the following:

f.3.b.1. A Full-Width Half-Maximum (FWHM) spot size smaller than 65 nm and an image placement less than 17 nm (mean + 3 sigma); *or*

f.3.b.2. [Reserved]

f.3.b.3. A second-layer overlay error of less than 23 nm (mean + 3 sigma) on the mask;

f.4. Equipment designed for device processing using direct writing methods, having all of the following:

f.4.a. A deflected focused electron beam; *and*

f.4.b. Having any of the following:

f.4.b.1. A minimum beam size equal to or smaller than 15 nm; *or*

f.4.b.2. An overlay error less than 27 nm (mean + 3 sigma);

f.5. Imprint lithography equipment having an overlay accuracy less (better) than 1.5;

f.6. Commodities not specified by 3B001.f.1, designed or modified to perform all of the following in or with deep-ultraviolet immersion photolithography equipment:

f.6.a. Decrease the minimum resolvable feature specified by 3B001.f.1.b; *and*

f.6.b. Decrease the maximum 'dedicated chuck overlay' of a deep-ultraviolet immersion lithography tool below or equal to 1.5 nm.

g. Masks and reticles, designed for integrated circuits controlled by 3A001;

h. Multi-layer masks with a phase shift layer not specified by 3B001.g and designed to be used by lithography equipment having a light source wavelength less than 245 nm;

Note: *3B001.h does not control multi-layer masks with a phase shift layer designed for the fabrication of memory devices not controlled by 3A001.*

N.B.: *For masks and reticles, ''specially designed'' for optical sensors, see 6B002.*

i. Imprint lithography templates designed for integrated circuits by 3A001;

j. Mask ''substrate blanks'' with multilayer reflector structure consisting of molybdenum and silicon, and having all of the following:

j.1. ''Specially designed'' for ''Extreme Ultraviolet'' (''EUV'') lithography; *and*

j.2. Compliant with SEMI Standard P37;

k. Equipment designed for ion beam deposition or physical vapor deposition of a multi-layer reflector for ''EUV'' masks;

l. ''EUV'' pellicles;

m. Equipment for manufacturing ''EUV'' pellicles;

n. Equipment designed for coating, depositing, baking, or developing photoresist formulated for ''EUV'' lithography;

o. [Reserved]

p. Removal and cleaning equipment as follows:

p.1. [Reserved]

p.2. Single wafer wet cleaning equipment with surface modification drying; *or*

p.3. [Reserved]

p.4. Equipment designed for single wafer cleaning using supercritical CO_2 or sublimation drying;

q. ''EUV'' masks and ''EUV'' reticles, designed for integrated circuits, not specified by 3B001.g, and having a mask ''substrate blank'' specified by 3B001.j; *or*

Technical Notes: *For the purposes of 3B001.q, masks or reticles with a mounted pellicle are considered masks and reticles.*

r. Equipment designed for EUV 'pattern shaping.'

Technical Note: *For the purposes of 3B001.r, 'pattern shaping' is a deposition or removal process used to improve overall patterning by reshaping or trimming patterns produced using EUV lithography with non-vertical directed particles including ions, neutral particles, clusters, radicals, or light.*

* * * * *

3B993 Specified semiconductor manufacturing equipment as follows (see list of items controls), and ''specially designed'' ''components'' and ''accessories'' therefor.

License Requirements

Reason for Control: RS, AT

Control(s)	*Country chart (see Supp. No. 1 to part 738)*
RS applies to entire entry.	See § 742.6(a)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

LVS: N/A
GBS: N/A

List of Items Controlled

Related Controls: (1) See ECCNs 3D993 and 3E993 for associated ''software'' and ''technology'' controls. (2) For additional controls that apply to this ECCN, see also § 744.11(a)(2)(v) and § 744.23(a)(4) of the EAR.
Related Definitions: N/A
Items:

a. [Reserved]

b. Semiconductor wafer fabrication equipment for 300 mm wafers designed for ion implantation and having any of the following:

b.1. Equipment designed for plasma doping, having all of the following:

b.1.a. One or more Radio Frequency (RF) power source(s);

b.1.b. One or more pulsed DC Power Source; *and*

b.1.c. One or more n-type or p-type dopant implants.

b.2 [Reserved]

c. Etch equipment as follows:

c.1. Equipment designed or modified for anisotropic etching of dielectric materials and enabling the fabrication of high aspect ratio features with aspect ratio greater than 30:1 and a lateral dimension on the top surface of less than 100 nm, and having all of the following:

c.1.a. Radio Frequency (RF) power source(s) with at least one pulsed RF output; *and*

c.1.b. One or more fast gas switching valve(s) with switching time less than 300 milliseconds.

Note: *3B993.c.1 includes etching by 'radicals', ions, sequential reactions, or non-sequential reaction.*

Technical Note: *For the purposes of the Note to 3B993.c.1, 'radical' is defined as an atom, molecule, or ion that has an unpaired electron in an open electron shell configuration.*

c.2. Equipment, not specified by 3B993.c.1, designed for anisotropic etching of dielectric material and enabling the fabrication of high aspect ratio features having all of the following:

c.2.a. An aspect ratio greater than 30:1; *and*

c.2.b. A lateral dimension on the top surface of less than 40 nm.

Note: *3B993.c.2 does not apply to equipment designed for wafer diameters less than 300 mm.*

c.3. Equipment, not specified by 3B001.c.1.c, designed or modified for anisotropic dry etching, having all of the following:

c.3.a. Radio Frequency (RF) power source(s) with at least one pulsed RF output;

c.3.b. One or more fast gas switching valve(s) with switching time less than 500 milliseconds; *and*

c.3.c. Electrostatic chuck with greater than or equal to 10 individually controllable variable temperature elements.

d. Semiconductor manufacturing deposition equipment as follows:

d.1. Equipment designed, not specified by 3B001.d.14, for deposition assisted by remotely generated 'radicals', enabling the fabrication of a silicon (Si) and carbon (C) containing film, and having all of the following properties of the deposited film:

d.1.a. A dielectric constant (k) of less than 5.3;

d.1.b. In features with an aspect ratio greater than 5:1 with lateral openings of less than 70 nm; *and*

d.1.c. A feature-to-feature pitch of less than 100 nm.

d.2. Equipment designed for deposition of a film, containing silicon and carbon, and having a dielectric constant (k) of less than 5.3, into lateral openings having widths of less than 70 nm and aspect ratios greater than 5:1 (depth: width) and a feature-to-feature pitch of less than 100 nm, while maintaining the wafer substrate at a temperature greater than 400 °C and less than 650 °C, and having all of the following:

d.2.a. Boat designed to hold multiple vertically stacked wafers;

d.2.b. Two or more vertical injectors; and

d.2.c. A silicon source and propene are introduced to a different injector than a nitrogen source or an oxygen source.

d.3. Equipment designed for chemical vapor deposition of a carbon material layer with a density more than 1.6 g/cm^3.

d.4. Deposition equipment, not specified by 3B001.d.19, having direct-liquid injection of more than two metal precursors, designed or modified to deposit a conformal dielectric film with a dielectric constant (K) greater than 35 in features with aspect ratio greater than 50:1 in a single deposition chamber.

e. [Reserved]

f. Lithography commodities as follows:

f.1. Align and expose step and repeat (direct step on wafer) or step and scan (scanner) lithography equipment for wafer processing using photo-optical or X-ray methods and having all of the following:

f.1.a. [Reserved]

f.1.b. A light source wavelength equal to or longer than 193 nm and having all of the following:

f.1.b.1 The capability to produce a pattern with a 'Minimum Resolvable Feature size' ('MRF') of 45 nm or less; *and*

f.1.b.2. A maximum 'dedicated chuck overlay' value greater than 1.50 nm and less than or equal to 2.40 nm.

Technical Notes for paragraph 3B993.f.1:

1. The 'Minimum Resolvable Feature size' ('MRF') is calculated by the following formula:

$$'MRF' = \frac{(\text{an exposure light source wavelength in nm}) \times (\text{K factor})}{\text{maximum numerical aperture}}$$

where, for the purposes of 3B993.f.1, the K factor = 0.25.

'MRF' is also known as resolution.

2. 'Dedicated chuck overlay' is the alignment accuracy of a new pattern to an existing pattern printed on a wafer by the same lithographic system. 'Dedicated chuck overlay' is also known as single machine overlay.

f.2. Imprint lithography equipment having an overlay accuracy above 1.5 nm and less (better) than or equal to 4.0 nm.

f.3. Commodities designed or modified to increase the number of wafers processed per hour, averaged over any time interval, by greater than 1%, of equipment specified in 3B001.f.1 or 3B993.f.1.

f.4. Commodities not specified by 3B993.f.1 designed or modified to perform all of the following in or with deep-ultraviolet immersion photolithography equipment:

f.4.a. Decrease the minimum resolvable feature specified by 3B993.f.1.b.1; and

f.4.b. Decrease the maximum 'dedicated chuck overlay' of deep-ultraviolet immersion lithography equipment above 1.5 nm and below or equal to 2.4 nm.

g. through n. [Reserved]

o. Annealing equipment designed for 300 mm wafers as follows:

o.1 Annealing equipment, operating in a vacuum (equal to or less than 0.01 Pa) environment, performing any of the following:

o.1.a Reflow of copper (Cu) to minimize or eliminate voids or seams in copper (Cu) metal interconnects; *or*

o.1.b Reflow of cobalt (Co) or tungsten (W) fill metal to minimize or eliminate voids or seams;

o.2. Equipment designed to heat a semiconductor wafer to a temperature greater than 1000 °C (1832 °F) for a 'duration' less than 2 ms.

Technical Note: *For the purposes of 3B993.o.2, 'duration' is the period above stated temperature.*

p. Removal and cleaning equipment as follows:

p.1. Equipment designed for removing polymeric residue and copper oxide (CuO) film and enabling deposition of copper (Cu) metal in a vacuum (equal to or less than 0.01 Pa) environment.

p.2. [Reserved]

p.3. Equipment designed for dry surface oxide removal preclean or dry surface decontamination.

Note to 3B993.p.1 and p.3: *These controls do not apply to deposition equipment.*

q. Inspection and metrology equipment as follows:

q.1. Patterned wafer defect metrology or patterned wafer defect inspection equipment, designed or modified to accept wafers greater than or equal to 300 mm in diameter, and having all of the following:

q.1.a. Designed or modified to detect defects having a size equal to or less than 21 nm; *and*

q.1.b. Having any of the following:

q.1.b.1. A light source with an optical wavelength less than 400 nm;

q.1.b.2. An electron-beam source with a resolution less (better) than or equal to 1.65 nm;

q.1.b.3. A Cold Field Emission (CFE) electron-beam source; *or*

q.1.b.4. Two or more electron-beam sources.

q.2. Metrology equipment as follows:

q.2.a. Stand-alone equipment designed to measure wafer shape parameters prior to lithography exposure and utilize measurements to improve overlay or focus of a deep ultraviolet (DUV) lithography system having an immersion lens having a numerical aperture more than 1.3 or an Extreme Ultraviolet lithography (EUV) system; *or*

q.2.b. Metrology equipment designed to measure focus or overlay after resist development or after etch on product wafers using image-based overlay or diffraction-based measurements techniques, with an overlay measurement accuracy less (better) than or equal to 0.5 nm having any of the following:

q.2.b.1 designed for integration to a 'track'; *or*

q.2.b.2 'fast wavelength switching functionality';

Technical Notes:

1. For the purposes of 3B993.q.2, a 'track' is equipment designed for coating and developing photoresist formulated for lithography.

2. For the purposes of 3B993.q.2, 'fast wavelength switching functionality' is defined as having the ability the change the measurement wavelength and acquire a measurement in less than 25 ms.

* * * * *

3B994 Semiconductor manufacturing equipment that enables ''advanced-node integrated circuit'' production, as follows (see list of items controls), and ''specially designed'' ''components'' and ''accessories'' therefor.

License Requirements

Reason for Control: RS, AT

Control(s)	*Country chart (see Supp. No. 1 to part 738)*
RS applies to entire entry.	See § 742.6(a)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

LVS: N/A
GBS: N/A

Special Conditions for STA

STA: License Exception STA may not be used to ship or transmit commodities specified in this ECCN to any of the destinations listed in Country Group A:5 or A:6 (See supplement no.1 to part 740 of the EAR).

List of Items Controlled

Related Controls: (1) See ECCNs 3D994 and 3E994 for associated software and technology controls. (2) For additional controls that apply to this ECCN, see also § 744.11(a)(2)(v) and § 744.23(a)(4) of the EAR.

Related Definitions: N/A

Items:

Note for 3B994: *Equipment specified in this ECCN 3B994 are limited to equipment designed for volume production, such as equipment designed to accept a SEMI standard wafer carrier such as a 200 mm or larger Front Opening Unified Pod or be connected to a multi-chamber wafer handling system.*

a. [Reserved]

b. Semiconductor wafer fabrication equipment designed for ion implantation of 300mm wafers as follows:

b.1. [Reserved]

b.2. Ion implantation equipment as follows:

b.2.a. Having all of the following:

b.2.a.1. Beam current greater than 1uA and less than 5mA; *and*

b.2.a.2. Beam energy greater than 5 keV and less than 300 keV; *or*

b.2.b. Having all of the following:

b.2.b.1. Beam current greater than 5 mA; *and*

b.2.b.2. Beam energy less than 5 keV; *or*

b.2.c. Having angular accuracy equal to or less (better) than 0.1 degrees.

c. through p. [Reserved]

q. Inspection and metrology equipment as follows:

q.1. and q.2. [Reserved]

q.3. Optical thin film metrology equipment or optical critical dimension metrology equipment designed for 300mm wafers and containing software designed for measuring non-planar transistors.

* * * * *

3D992 ''Software'' for the ''development'' or ''production'' of commodities specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, or 3B002.c and ''software'' as follows (see List of Items Controlled).

License Requirements

Reason for Control: NS, RS, AT

Control(s)	*Country chart (see Supp. No. 1 to part 738)*
NS applies to the entire entry.	To or within Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR. *See* § 742.4(a)(4) of the EAR.
RS applies to the entire entry.	To or within Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR. See § 742.6(a)(6)(i) of the EAR.
NS applies to ''software'' for equipment controlled by 3B001.c.1.a or c.1.c.	Worldwide control. See § 742.4(a)(5) and (b)(10) of the EAR.
RS applies to ''software'' for equipment controlled by 3B001.c.1.a or c.1.c.	Worldwide control. See § 742.6(a)(10) and (b)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

TSR: N/A

IEC: Yes, for ''software'' for equipment controlled by 3B001.c.1.a and 3B001.c.1.c, see § 740.2(a)(22) and § 740.24 of the EAR.

Special Conditions for STA

STA: License Exception STA may not be used to ship or transmit ''software'' specified in this ECCN to any of the destinations listed in Country Group A:5 or A:6 (See supplement no.1 to part 740 of the EAR).

List of Items Controlled

Related Controls: For additional controls that apply to this ECCN, see also § 744.11(a)(2)(v) and (a)(3) and § 744.23(a)(4)(iii) of the EAR.

Related Definitions: N/A

Items:

a. ''Software'' ''specially designed'' for the ''development'' or ''production,'' of commodities specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r, or 3B002.c.

b. 'Electronic Computer-Aided Design' ('ECAD') ''software'' designed for the integration of multiple dies into a 'multi-chip' integrated circuit, and having all of the following:

b.1. Floor planning; *and*

b.2. Co-design or co-simulation of die and package.

Technical Note: *For the purposes of 3D992.b, 'multi-chip' includes multi-die and multi-chiplet.*

c. ''Software'' not specified by 3D992.a designed or modified to perform all of the following in or with deep-ultraviolet immersion photolithography equipment:

c.1. Decrease the minimum resolvable feature specified by 3B001.f.1.b; and

c.2. Decrease the maximum 'dedicated chuck overlay' of deep-ultraviolet immersion lithography equipment below or equal to 1.5 nm.

3D993 ''Software'' for the ''development'' or ''production'' of commodities specified in 3B993 and ''software'' as follows (see List of Items Controlled).

License Requirements

Reason for Control: RS, AT

Control(s)	*Country chart (see Supp. No. 1 to part 738)*
RS applies to entire entry.	See § 742.6(a)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

TSR: N/A

Special Conditions for STA

STA: License Exception STA may not be used to ship or transmit ''software'' specified in this ECCN to any of the destinations listed in Country Group A:5 or A:6 (see supplement no.1 to part 740 of the EAR).

List of Items Controlled

Related Controls: For additional controls that apply to this ECCN, see also § 744.11(a)(2)(v) and (a)(3) and § 744.23(a)(4)(iii) of the EAR.

Related Definitions: N/A

Items:

a. ''Software'' ''specially designed'' for the ''development'' or ''production'' of commodities specified in 3B993.

b. 'Electronic Computer-Aided Design' ('ECAD') ''software'' designed or modified for the ''development'' or ''production'' of integrated circuits using multipatterning.

c. 'Computational lithography' ''software'' designed or modified for the ''development'' or ''production'' of patterns on DUV lithography masks or reticles.

Technical Note: *For the purposes of 3D993, 'computational lithography' is the use of computer modelling to predict, correct, optimize and verify imaging performance of the lithography process over a range of patterns, processes, and system conditions.*

d. ''Software'' designed or modified to increase the number of wafers processed per hour, averaged over any time interval, by greater than 1%, of equipment specified in 3B001.f.1 or 3B993.f.1.

e. ''Software'' not specified by 3D993.a designed or modified to perform all of the following in or with deep-ultraviolet immersion photolithography equipment:

e.1. Decrease the minimum resolvable feature specified by 3B993.f.1.b.1; *and*

e.2. Decrease the maximum 'dedicated chuck overlay' of deep-ultraviolet immersion lithography equipment above 1.5 nm and below or equal to 2.4 nm.

3D994 ''Software'' ''specially designed'' for the ''development'' or ''production'' of commodities specified in 3B994 and ''software'' as follows (see List of Items Controlled).

License Requirements

Reason for Control: RS, AT

Control(s)	*Country chart (see Supp. No. 1 to part 738)*
RS applies to entire entry.	See § 742.6(a)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

TSR: N/A

Special Conditions for STA

STA: License Exception STA may not be used to ship or transmit ''software'' specified in this ECCN to any of the destinations listed in Country Group A:5 or A:6 (see supplement no. 1 to part 740 of the EAR).

List of Items Controlled

Related Controls: For additional controls that apply to this ECCN, see also § 744.11(a)(2)(v) and (a)(3) and § 744.23(a)(4)(iii) of the EAR.

Related Definitions: N/A

Items: The list of items controlled is contained in the ECCN heading.

* * * * *

3E992 ''Technology'' for the ''production'' or ''development'' of commodities specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r; and 3B002.c; and ''technology'' as follows (see List of Items Controlled).

License Requirements

Reason for Control: NS, RS, AT

Control(s)	Country chart (see Supp. No. 1 to part 738)
NS applies to the entire entry.	To or within Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR. See § 742.4(a)(4) of the EAR.
RS applies to the entire entry.	To or within Macau or a destination specified in Country Group D:5 of supplement no. 1 to part 740 of the EAR. See § 742.6(a)(6)(i) of the EAR.
NS applies to ''software'' for equipment controlled by 3B001.c.1.a or c.1.c.	Worldwide control. See § 742.4(a)(5) and (b)(10) of the EAR.
RS applies to ''software'' for equipment controlled by 3B001.c.1.a or c.1.c.	Worldwide control. See § 742.6(a)(10) and (b)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

TSR: N/A

IEC: Yes, for ''technology'' for equipment controlled by 3B001.c.1.a, and 3B001.c.1.c, see § 740.2(a)(22) and § 740.24 of the EAR.

Special Conditions for STA

STA: License Exception STA may not be used to ship or transmit ''technology'' specified in this ECCN to any of the destinations listed in Country Group A:5 or A:6 (see supplement no. 1 to part 740 of the EAR).

List of Items Controlled

Related Controls: N/A

Related Definitions: N/A

Items:

a. ''Technology'' ''specially designed'' for the ''development'' or ''production'' of commodities specified in 3B001.a.4, c, d, f.1, f.5, f.6, k to n, p.2, p.4, r; or 3B002.c.

b. ''Technology'' not specified by 3E992.a designed or modified to perform all of the following in or with deep-ultraviolet immersion photolithography equipment:

b.1. Decrease the minimum resolvable feature specified by 3B001.f.1.b; *and*

b.2. Decrease the maximum 'dedicated chuck overlay' of deep-ultraviolet immersion lithography equipment below or equal to 1.5 nm.

3E993 ''Technology'' for the ''development'' or ''production'' of commodities specified in 3B993; and ''technology'' as follows (see List of Items Controlled).

License Requirements

Reason for Control: RS, AT

Control(s)	Country chart (see Supp. No. 1 to part 738)
RS applies to entire entry.	See § 742.6(a)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

TSR: N/A

Special Conditions for STA

STA: License Exception STA may not be used to ship or transmit ''technology'' specified in this ECCN to any of the destinations listed in Country Group A:5 or A:6 (see supplement no. 1 to part 740 of the EAR).

List of Items Controlled

Related Controls: For additional controls that apply to this ECCN, see also § 744.11(a)(2)(v) and (a)(3) and § 744.23(a)(4)(iii) of the EAR.

Related Definitions: N/A

Items:

a. ''Technology'' ''specially designed'' for the ''development'' or ''production'' of commodities specified by 3B993.

b. ''Technology'' designed or modified to increase the number of wafers processed per hour, averaged over any time interval, by greater than 1%, of equipment specified in 3B001.f.1 or 3B993.f.1.

c. ''Technology'' not specified by 3E993.a designed or modified to perform all of the following in or with deep-ultraviolet immersion photolithography equipment:

c.1. Decrease the minimum resolvable feature specified by 3B993.f.1.b.1; *and*

c.2. Decrease the maximum 'dedicated chuck overlay' of a deep-ultraviolet immersion lithography equipment above 1.5 nm and below or equal to 2.4 nm.

3E994 ''Technology'' ''specially designed'' for the ''development'' or ''production'' of commodities specified in 3B994 and ''technology'' as follows (see List of Items Controlled).

License Requirements

Reason for Control: RS, AT

Control(s)	Country chart (see Supp. No. 1 to part 738)
RS applies to entire entry.	See § 742.6(a)(11) of the EAR.
AT applies to entire entry	AT Column 1.

List Based License Exceptions (See Part 740 for a Description of All License Exceptions)

TSR: N/A

Special Conditions for STA

STA: License Exception STA may not be used to ship or transmit ''technology'' specified in this ECCN to any of the destinations listed in Country Group A:5 or A:6 (see supplement no. 1 to part 740 of the EAR).

List of Items Controlled

Related Controls: For additional controls that apply to this ECCN, see also § 744.11(a)(2)(v) and (a)(3) and § 744.23(a)(4)(iii) of the EAR.

Related Definitions: N/A

Items: The list of items controlled is contained in the ECCN heading.

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Matthew S. Borman,

Principal Deputy Assistant Secretary for Strategic Trade and Technology Security.

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