NBSIR 79-1591

Semiconductor Technology Program Progress Briefs

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Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, D.C. 20234

January 1979

Prepared for

The Defense Advanced Research Projects Agency
The National Bureau of Standards
The Division of Electric Energy Systems, Department of Energy
The Division of Solar Technology, Department of Energy
The Defense Nuclear Agency
The Charles Stark Draper Laboratory
The Army Electronics Research and Development Command
The Air Force Avionics Laboratory
Navy Material Command
Naval Weapons Support Center

ABSTRACT — This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include studies of: laser annealing of low-fluence implants in silicon; analysis techniques for spreading resistance profiling measurements; Hall effect measurements in two-layer structures; incorporation of hydrogen and hydroxyl impurities in silicon dioxide films; an integrated gated-diode electrometer test structure; defect-density profiling by constant-capacitance deep-level transient spectroscopy; and a spatial integrity test pattern for electrical measurement of intra- and inter-die line-width variations. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

SEMICONDUCTOR TECHNOLOGY PROGRAM

TABLE OF CONTENTS

KEY WORDS: Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

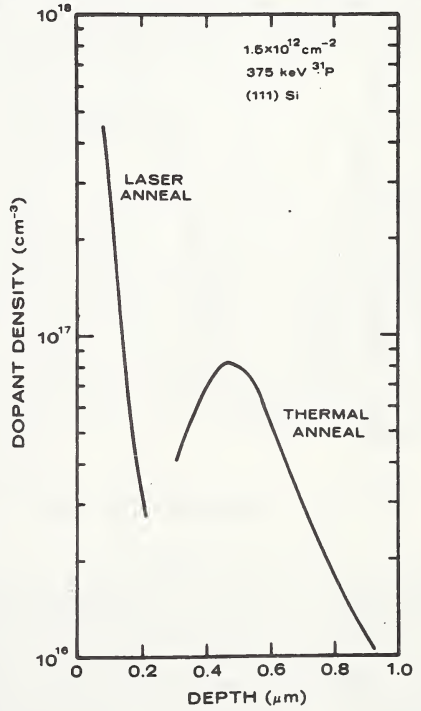
Preface

This report covers results of work during the forty-first quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Division of Solar Technology, Department of Energy; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 7. The Army Electronics R&D Command; 8. The Air Force Avionics Laboratory; 9. The Navy Material Command; and 10. The Naval Weapons Support Center.

This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

Laser Annealing in Silicon

Low-fluence ion implantation is widely used in silicon device fabrication for such purposes as threshold voltage adjustment in MOS transistors and as base implants for bipolar transistors. These implants require higher annealing temperatures for electrical activation of the dopant species than higher fluence implants which drive the surface amorphous. A study was undertaken to investigate the effectiveness of laser irradiation for annealing damage from such low-fluence implants. Silicon wafers were implanted with boron or phosphorus ions to fluences of 1.5×10^{12} cm^{-2} at energies of several hundred kilovolts. Part of each wafer was annealed for 30 min in dry nitrogen at 700°C or 800°C. The remaining part was subjected to single-pulse laser annealing at integrated energy densities ranging from 0.7 to 2.8 J/cm^2. The laser used was a flashlamp-excited dye laser tuned to a wavelength of 600 nm which had a pulse duration of about 1 μs with a roughly triangular waveform peaked at about 230 ns. The electrical activation of the annealed areas was examined with capacitance-voltage profiling of Schottky-barrier diodes formed after annealing. In the boron-implanted wafers, there was significant boron activation in the laser-annealed areas with peak dopant densities 25 to 100% of those obtained from thermal annealing alone; for neither laser nor thermal annealing did significant redistribution occur. In the phosphorus-implanted wafers, areas in which laser irradiation was sufficient to cause electrical activation exhibited dopant segregation at the surface similar to zone refining, as shown in the accompanying figure. At the highest power densities employed, surface morphology characteristic of melting and regrowth could be detected by Nomarski interference microscopy. Examination of the phosphorus-implanted wafers with the scanning electron microscope in the charge collection mode indicated the presence of electrically active defect structures in both unannealed and thermally annealed areas, but no defect structures could be detected in laser-annealed areas that had melted. These results imply that temperatures near or above the melting point must be reached during laser annealing to activate boron or phosphorus implanted into silicon at low fluences and suggest that laser-induced melt and regrowth removes distinct electrically active defect structures from the implanted regions. In addition, these results suggest that

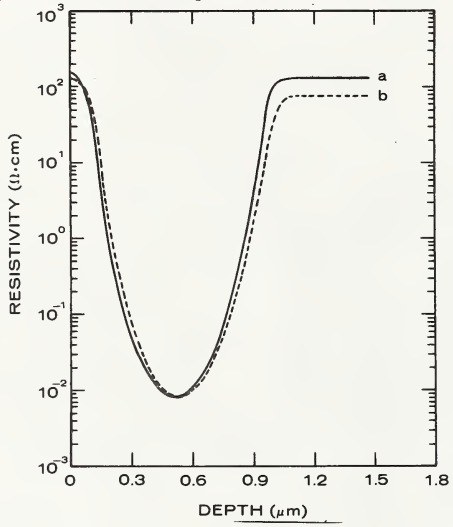


Capacitance-voltage profiles of a phosphorus-implanted silicon wafer characteristic of thermally annealed or laser-annealed areas of the wafer, illustrating segregation of phosphorus in the surface region of the laser-annealed areas.

the laser pulse duration or shape may be responsible for the dopant segregation seen in these studies. These results differ markedly from the solute trapping regrowth mechanisms seen for short pulse (50 ns) ruby or Nd:YAG lasers. [Sponsor: 2] (D. R. Myers,* P. Roitman,* S. Mayo, x3625)

Spreading Resistance Algorithms

A program has been written which computes model spreading resistance data from input profile resistivities. The program is based upon the Schumann-Gardner equation for the correction factor and the Choo recursion relation for the kernel of the correction factor integral. Model resistivity profiles for Gaussian diffusions and implants (both single and double peak) were used in the program to generate spreading resistance data for these profiles. The calculated spreading resistance values were analyzed according to both Dutton-D'Avanzo's multilayer algorithm and Dickey's local-slope algorithm, and the results were compared with the original input resistivities. The multilayer results agreed with the original sheet resistance to within less than 1%, and the local-slope results agreed to within approximately 10%. In general, the point-by-point agreement between the calculated and measured resistivities was not as good as the sheet resistance agreement. The comparison of the original resistivities with those predicted by the multilayer analysis and the local-slope analysis indicates that the multilayer resistivities differ from the original resistivities by at most 10%, whereas the local-slope resistivities differ from the original resistivities by significantly greater amounts, as much as a factor of 2. The differences between the original and multilayer resistivities are in most part probably due to the choice of the upper limit of 10 μm^{-1} for the Schumann-Gardner integrals, as use of an upper limit of 20 μm^{-1} decreases the difference between the original and multilayer resistivities. The differences between the local-slope resistivities and the original resistivities are due to the inaccuracy of the relation between the correction factor and the local slope. Despite this, use of the local-slope algorithm results in a reasonably satisfactory profile, as can be seen in the accompanying figure. [Sponsor: 1] (J. H. Albers, x3625)



Model resistivity profiles for a 200-keV boron implant (Gaussian approximation) into 110 Ω·cm p-type silicon. The original resistivity profile and the resistivity profile computed from calculated spreading resistance data using the multilayer algorithm, which are indistinguishable on this scale, are given by the solid curve. The resistivity profile computed from the calculated spreading resistance data using the local-slope algorithm is given by the dashed curve.

Hall Effect in Two-Layer Structures

A technique was developed for measuring resistivity and Hall coefficient of epitaxial layers of silicon on substrates of the opposite conductivity type for cases where the junction at the interface has a significant leakage current and therefore does not effectively iso-

*NBS-NRC Postdoctoral Research Associate..

late the two regions. In this technique, the measurements are made simultaneously on both the epitaxial layer and its substrate, the interface impedance is measured, and the interaction between the two regions is modeled and taken into account. This technique can be used not only to measure the unperturbed resistivity and Hall coefficient of each layer separately, but also to verify those cases in which the perturbing effects of a high resistivity substrate are negligible, thus justifying conventional measurements on the epitaxial layer. The technique was applied to measure the properties of indium-doped epitaxial layers on indium-doped or undoped bulk-grown substrates at room temperature and at 77 K. The epitaxial layers were found to contain a dominating *n*-type impurity with an activation energy characteristic of phosphorus. This impurity presumably arose from undesired contamination in the epitaxial growth system used to produce these specimens. [Sponsor: 7] (R. D. Larrabee and W. R. Thurber, x3625)

Impurities in Silicon Dioxide Films

Analysis was completed of the mechanisms through which hydrogen and hydroxyl impurities become incorporated into thin, thermally grown silicon dioxide films prepared in nominally dry oxidation atmospheres enclosed in resistance-heated fused silica or silicon tubes. This work indicates that only 1 ppm water contamination in the oxidation atmosphere is sufficient to account for the hydrogen and hydroxyl contamination observed experimentally in the oxide films. Trace water and hydrocarbon contamination in the semiconductor grade oxygen is a major source of this water contamination in the oxidation atmosphere. In addition, diffusion of water vapor from the surrounding ambient through the oxidation tube also contributes water contamination to the oxidation atmosphere. In this regard, use of a polycrystalline silicon oxidation tube is preferred over a fused silica tube due to the inherent water gettering action of silicon at oxidation temperatures. [Sponsor: 5] (S. Mayo, x3625)

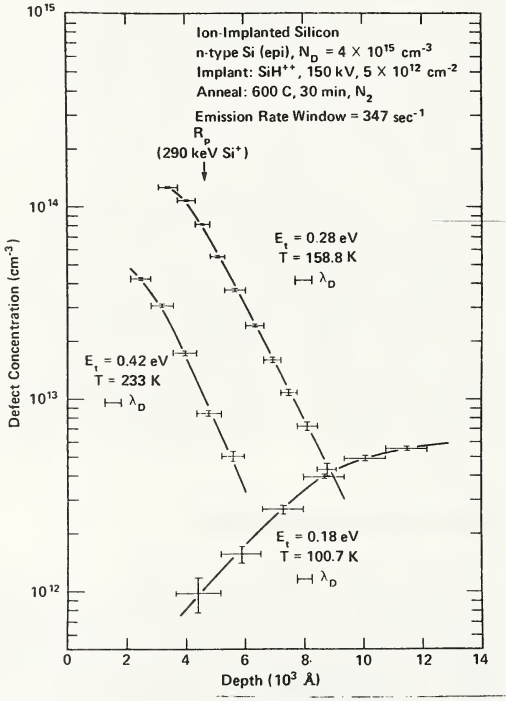
Integrated Gated-Diode Electrometer

Detailed study of the integrated gated-diode electrometer test structure has provided an explanation for the deviations between the leakage currents derived from the amplifier output voltage signal and the leakage measured directly from the diode under test. The dominant deviations can be accounted for by considering all parasitic capacitance sources. Sources of parasitic capacitance include the capacitance between the input FET gate and the inversion layer and the overlap capacitance between the input FET gate and its source and drain, etc. These capacitances are especially important in the gated-diode electrometer test structure because its metrology involves determining the leakage current from the decay voltage across the capacitance of the diode junction. Because the diode capacitance is a depletion capacitance, parasitic capacitors which are gate oxide capacitors (the diode gate-to-junction overlap capacitance, for example) could have unexpectedly large values even though they may be very small in area. This is because the gate oxide thickness is much less than the junction depletion depth. [Sponsor: 6] (G. P. Carver, x3541)

Defect-Density Profiling

A method has been developed at Xerox Palo Alto Research Center to obtain spatial depth profiles of electronic defects in semiconductors from deep-level spectroscopic measurements performed in the constant-capacitance mode. Deep-level transient spectroscopy (DLTS), performed in either the conventional capacitance-transient mode or the constant-capacitance mode, provides the energy levels of defect states in the band gap of the semiconductor. The double-correlation DLTS technique

(DDLTS) is used to define a narrow spatial observation window for defect profiling. However, in the analysis of capacitance-transient DDLTS data, specific approximations are required to deal with the change with time of the semiconductor depletion width during the transient response to a charging pulse. In the constant-capacitance mode, the depletion width is held constant by dynamically varying the applied voltage during the transient response, thus permitting more accurate measurement of defect profiles at high trap densities. The method was applied to measurement of damage profiles of silicon implanted into silicon at low fluence. Three defect levels were observed. The densities of the defects with energies 280 and 420 meV below the conduction band edge decrease monotonically with distance from the silicon surface. These levels are ascribed to residual implantation damage, as suggested by their rapid decay over a depth comparable to the projected range for Si^+ implanted at 290 keV. The third level, 180 meV below the conduction band edge, has been identified with the A center, a defect complex consisting of substitutional oxygen adjacent to a silicon vacancy. The density of the A centers increases over the same range as the damage centers decrease in density. This may be related to the annealing kinetics of implantation damage. [Sponsor: 1] (K. F. Galloway,* x3625)



Spatial depth profiles for three defect levels in silicon implanted with silicon. With each profile is listed the trap energy E_t, the measurement temperature T, and the extrinsic Debye length λ_D. The horizontal bars mark the computed intervals over which the average defect concentrations were measured. Note: 10^3 Å = 0.1 μm.

Line-Width Variation Measurements

A simple, single-level test pattern, NBS-21, has been designed and fabricated to measure the periodic and random variations in line width and sheet resistance across a die and across a wafer. The pattern, which consists of an 8 by 15 array of identical cross-bridge sheet resistors, is repeated across the entire wafer at 200-mil (5.08-mm) intervals. A two-inch diameter wafer contains 53 such arrays or over 6300 sheet resistors. The repeated pattern is etched on a metal film evaporated on an oxidized silicon wafer, and the line width of each of the sheet resistors is measured electrically. Preliminary results obtained with this spatial integrity test device suggest that variations due to the characteristics of the photolithographic systems used to both fabricate the masks and pattern the wafer can be observed. [Sponsors: 1,8] (L. W. Linholm, x3541)

New Topics . . .

Infrared Detector Materials — An infrared laser-scan technique for measuring the uniformity of photoresponse over the wafer surface is being explored to determine its suitability for use as a practical method for screening out

*NBS Contact.

starting wafers of indium-doped silicon which, if processed, would yield unacceptable detector arrays. Since measurement time and cost are important considerations, the technique is being studied at liquid nitrogen temperature instead of the lower operating temperature of indium-doped infrared imaging arrays. It was found that the magnitude of the photoconductive signal is severely limited by the fact that very small amounts of bias current and laser light produce temperature differences within the wafer that can cause nonuniformities in otherwise homogeneous wafers. Since noise becomes a potential problem for small signals, the experiments presently in progress are concerned with the feasibility of using mechanical point contacts instead of more ideal, but less practical, alloyed metallic contacts at the edge of the wafer. If the various problems can be resolved, the photoconductivity scan, when coupled with a measurement of the infrared absorption to determine the uniformity of the indium density, is expected to provide a practical screening method. Although the present emphasis is directed toward indium-doped silicon, the technique is not strongly material-dependent and can, in principle, be applied to wafers of any extrinsic or intrinsic photoconductive material. [Sponsor: 1] (R. D. Larrabee and W. R. Thurber, x3625)

Measurement of Moisture Levels in Semiconductor Device Packages — At the request of the industry, through JEDEC Committee JC-13 on Government Liaison, work has been undertaken to improve the between-laboratory precision in the measurement of internal moisture in hermetic semiconductor packages through development of well-characterized and stable transfer devices. The project is an interdisciplinary one which will be carried out with the participation of the humidity and mass spectroscopy groups at NBS. The problem is made particularly difficult by both the small quantities of water that are involved and the overbearing effect of surface processes. It is planned to systematically characterize the responses of a sampling of miniature aluminum oxide humisters; to incorporate such sensors, in multiple, within special reusable metal packages which are devoid of absorbents and which are initially equilibrated at given moisture concentrations; to make careful replicated correlations between humister measurements and mass spectroscopic measurements of the moisture levels in these packages, and at larger concentrations with ultrasensitive weighing and microsyringe techniques, which are absolute but less sensitive methods; and, finally, to use these well-characterized test packages as a transfer device for the evaluation and improvement of mass spectrometric measurement precision for both within-laboratory and between-laboratory comparisons. It is expected that this project will require about two years. [Sponsor: 9]

(S. Ruthberg, x3621)

Cross-Bridge Electrical Alignment Test Structure — Detailed evaluation has been initiated of a sheet resistor test structure for measuring the misalignment between the masks used to define a doped region and the contact window openings to that region, the sheet resistance of the doped region, and the width of the doped region. This structure is comprised of a cross-bridge sheet resistor test structure and an electrical alignment test structure; the combined structure requires 12 contact pads, one-third fewer than the two separate structures, and thus occupies significantly less space. A new test pattern, NBS-19, is being designed and when fabricated will provide the test vehicle for evaluating the new test structure. [Sponsor: 1]

(T. J. Russell, R. C. Frisch, and M. G. Buehler, x3541)

Update . . .

Changes were made in the Hall effect analysis program for calculating the electrical properties of silicon to obtain better agreement with experiment for high dopant densities and low tem-

peratures. In the mobility calculations, the effect of carrier-carrier scattering has been added and the expressions for ionized and neutral impurity scattering have been revised based on results obtained at the University of Florida. A routine for computing the reduction in activation energy as a function of dopant density and compensation was also added. As announced previously, the computer listing for this program is available on request. [Sponsor: 1]

(W. R. Thurber and R. D. Larrabee, x3625)

Work in Progress . . .

The interlaboratory evaluation of the procedure for measuring line widths in the 1- to 10-μm range on chrome photomasks in transmitted light is continuing. Although more than half the data scheduled to be taken has been submitted to NBS and analysis of the data has been initiated, considerable additional data must be obtained before the analysis can be completed. Consequently, it will not be possible to complete this evaluation by the end of 1978 as originally planned. [Sponsor: 1]

(J. M. Jerke, x2185)

Twenty sets of SRM 1522, Silicon Power Device Level Resistivity Standard, have been fabricated and measured. This new standard reference material is comprised of three 51-mm diameter slices of neutron-transmutation-doped (*n*-type) silicon with nominal resistivities (at room temperature) of 25, 75, and 180 Ω•cm. Each slice is nominally 25 mils (0.64 mm) thick. The resistivity values will be certified and the sets released for sale following completion of a two-operator, two-instrument experiment being conducted to estimate the measurement error. [Sponsor: 2]

(J. R. Ehrstein, x3625)

Comparisons have been made between carrier lifetime measurements made by the open circuit voltage decay (OCVD) and diode reverse recovery (DRR) methods on a commercially fabricated power rectifier wafer with approximately 150 processed devices. The OCVD measurements yielded lifetime values from 4.9 to 9.4 μs, about three-fourths of the values obtained with the DRR method. However, identical patterning of the measured wafer maps indicated that the two measurements tracked each other on a point-by-point basis. [Sponsor: 3]

(R. Y. Koyama, x3625)

Recent Publications . . .

*Grunthaner, F. J., and Maserjian, J., Chemical Structure of the Transition Region of the SiO_2/Si Interface, *The Physics of SiO_2 and Its Interfaces*, S. T. Pantelides, Ed., pp. 389-395 (Pergamon Press, New York, 1978).

*Helms, C. R., Johnson, N. M., Schwarz, S. A., and Spicer, W. E., Auger Sputter Profiling Studies of the Si-SiO_2 Interface, *The Physics of SiO_2 and Its Interfaces*, S. T. Pantelides, Ed., pp. 366-372 (Pergamon Press, New York, 1978).

Nyyssonen, D., Optical Linewidth Measurements on Wafers, *Proc. Soc. Photo-Optical Instrumentation Engineers* 135, *Developments in Semiconductor Microlithography III*, 115-119 (April 1978).

*Christou, A., Nelson, G., Jenkins, W., Davey, J. E., and Wilkens, N., Characterization of Semiconductor Wafer Defects by ASLEEP, SEM, and Scanning AES, *Scanning Electron Microscopy/1978*, Vol. 1, O'Hare, Illinois, April 17-21, 1978, pp. 273-282.

Sawyer, D. E., A Technique for Using An Optical Scanner to Reveal Solar Cell Defects, *Proc. 13th IEEE Photovoltaic Specialists Conference*, Washington, D.C., June 5-8, 1978, pp. 1249-1250.

*Weglein, R. D., and Wilson, R. G., Characteristic Material Signatures by Acoustic Microscopy, *Electron. Lett.* 14, 352-354 (8 June 1978).

Larrabee, R. D., "X" Levels in Indium-Doped Silicon, *Proc. IRIS Specialty Group Meeting*, Annapolis, Maryland, June 13-15, 1978, pp. 253-261.

*Johannessen, J. S., Spicer, W. E., Gib-

*Reports of Contract Research.

bons, J. F., Plummer, J. D., and Taylor, N. J., Observation of the Phosphorus Pile-Up at the SiO_2-Si Interface, *J. Appl. Phys.* 49, 4453-4458 (August 1978).

Sawyer, D. E., Kessler, H. K., and Schafft, H. A., Measurement Techniques for Solar Cells, Quarterly Report: January 1 to March 31, 1978, NBSIR 78-1513 (September 1978).

Harman, G. G., and Cannon, C. A., The Microelectronic Wire Bond Pull Test — How to Use It, How to Abuse It, *IEEE Trans. Components, Hybrids, and Manufacturing Technology* CHMT-1, 203-210 (September 1978).

Swyt, D. A., Rosberry, F. W., and Nyyssonen, D., Photomask Linewidth Measurement, *Circuits Manufacturing* 18 (9) 20 ff (September 1978).

*Li, S. S., The Dopant Density and Temperature Dependence of Hole Mobility and Resistivity in Boron-Doped Silicon, *Solid-State Electronics* 21, 1109-1117 (September 1978).

*Weglein, R. D., Gray Scale for Scanning Acoustic Microscopy, *Electron. Lett.* 14, 656-657 (28 September 1978).

*Stach, J., Das, M. G., and Tressler, R. E., Development of Measurement Techniques for Monitoring Chemical Purity of Materials Used in Digital IC Processing, NBS-GCR-78-134 (September 1978).

*Atalar, A., An Angular Spectrum Approach to Contrast in Reflection Acoustic Microscope, *J. Appl. Phys.* 49, 5130-5139 (October 1978).

Larrabee, R. D., and Thurber, W. R., Theory and Application of a Two-Layer Hall Technique, NBSIR 78-1553 (October 1978).

Scace, R. I., An Assessment of High-Power Thyristor Technology, NBSIR 78-1559 (October 1978).

Publications in Press . . .

Berning, D. W., *Semiconductor Measurement Technology:* A Reverse-Bias SOA Transistor Tester, NBS Spec. Publ. 400-54.

Bhar, T. N., Dat, R., Koyama, R. Y., and Galloway, K. F., Effect of Ionizing Radiation on Mobile-Ion Density in MOS Oxides, *Electron. Lett.*

Blackburn, D. L., and Berning, D. W., Some Effects of Base Current on Transistor Switching and Reverse-Bias Second-Breakdown, *Technical Digest, 1978 International Electron Devices Meeting,* Washington, D.C., December 4-6, 1978.

Buehler, M. G., Microelectronic Test Patterns for Use in Procuring LSICs, *Proc. Industry/Joint Services Automatic Test Conf. and Workshop,* San Diego, California, April 4-6, 1978.

Ehrstein, J. R., Two-Probe (Spreading Resistance) Measurements for Evaluation of Semiconductor Materials and Devices, *Nondestructive Evaluation of Semiconductor Materials and Devices,* NATO Advanced Study Institute, Frascati, Italy, September 18-30, 1978.

Galloway, K. F., VLSI Processing, Radiation, and Hardening, *IEEE Trans. Nucl. Sci.*

Gilsinn, D., and Kraft, R., *Semiconductor Measurement Technology:* DISTRIB I, An Impurity Redistribution Computer Program, NBS Spec. Publ. 400-57.

*Goodman, A. H., Extended Range MIS C(V) Measurement, A Technique for Monitoring Semiconductor Device Processing, NBS-GCR-78-155.

Harman, G. G., Nondestructive Tests Used to Insure the Integrity of Semiconductor Devices with Emphasis on Passive Acoustic Techniques, *Nondestructive Evaluation of Semiconductor Materials and Devices,* NATO Advanced Study Institute, Frascati, Italy, September 18-30, 1978.

Koyama, R. Y., *Semiconductor Measurement Technology:* A Wafer Chuck for Use Between -196° and 350°C, NBS Spec. Publ. 400-55.

Leedy, T. F., and Liu, Y. M., *Semiconductor Measurement Technology:* Microelectronic Processing Laboratory at NBS, NBS Spec. Publ. 400-53.

*Li, S. S., *Semiconductor Measurement Technology:* The Theoretical and Experimental Study of the Temperature and Dopant Density Dependence of the Hole

*Reports of Contract Research.

Mobility, Effective Mass, and Resistivity in Boron-Doped Silicon, NBS Spec. Publ. 400-47.

McCarthy, D., Acevedo, J., Stamps, B., Lonky, M., and Buehler, M. G., An Advanced Integrated Test Structure for High Speed Measurement of Generation Lifetime, *Proc. Govt. Microcircuit Applications Conf.*, Monterey, California, November 14-16, 1978.

Marsden, C. P., Tabulation of Published Data on Electron Devices of the U.S.S.R. Through December 1976, NBSIR 78-1564.

Mattis, R. L., and Doggett, M. R., A Microelectronic Test Pattern for Analyzing Problems Related to Automatic Wafer Probing and Probe Cards, *Solid State Technology*.

Mayo, S., and Evans, W. H., Development of Hydrogen and Hydroxyl Contamination in Thin SiO_2 Thermal Films, NBSIR 78-1558.

Myers, D. R., Koyama, R. Y., and Phillips, W. E., An Implantation Predeposition Technique for Deep Level Characterization, *Radiat. Eff.*

Myers, D. R., Roitman, P., and Mayo, S., Electrical Characterization of Low-Dose Ion Implanted Silicon Annealed with Microsecond Laser Pulses, *Proc. MRS Symp. on Laser-Solid Interactions and Laser Processing*, Boston, Massachusetts, November 28-December 1, 1978 (AIP Symposium Series).

Myers, D. R., and Wilson, R. G., Alignment Effects on Implantation Profiles in Silicon, *Radiat. Eff.*

Nyyssonen, D., and Jerke, J. M., Linewidth Measurement: From Fine Art to Science, *Technical Digest, 1978 International Electron Devices Meeting*, Washington, D.C., December 4-6, 1978.

Russell, T. J., and Maxwell, D. A., *Semiconductor Measurement Technology:* A Production-Compatible Microelectronic Test Pattern for Evaluating Photomask Misalignment, NBS Spec. Publ. 400-51.

Russell, T. J., Maxwell, D. A., Reimann, C. T., and Buehler, M. G., A Microelectronic Test Pattern for Measuring the Uniformity of an Integrated Circuit Fabrication Technology, *Proc. Govt. Microcircuit Applications Symp.*, Monterey, California, November 14-16, 1978.

Russell, T. J., Maxwell, D. A., Reimann, C. T., and Buehler, M. G., A Microelectronic Test Pattern for Measuring the Uniformity of an Integrated Circuit Fabrication Technology, *Solid State Technology*.

Sawyer, D. E., Kessler, H. K., and Schafft, H. A., Solar Cell Measurement Technique Development and Other Services, *Proc. DoE Annual Review for Advanced Materials R&D Branch*, Vail, Colorado, October 24-26, 1978.

Schafft, H. A., *Semiconductor Measurement Technology:* Reliability Technology for Cardiac Pacemakers III — A Workshop Report, NBS Spec. Publ. 400-50.

Schafft, H. A., Performance Criteria for Photovoltaic Power Conditioning, Control, and Storage, *Proc. DoE Photovoltaic Technology Development and Applications Program Review*, Arlington, Virginia, November 7-9, 1978.

*Schwarz, S. A., and Helms, C. R., A Geometrical Model of Sputtering, *Appl. Phys. Letters*.

*Sulouff, R. E., A Study of Leak Rate Versus Reliability of Hybrid Packages, *Proc. 1978 Internat. Microelectronics Symp.*, Minneapolis, Minnesota, September 25-27, 1978.

*Strausser, Y. E., Scheibner, E. J., and Johannessen, J. S., Observations of Al_2O_3 and Free Si in the Interface Between Al Films and SiO_2, *Thin Solid Films*.

*Weglein, R. D., and Wilson, R. G., An Acoustic Gray Scale for Scanning Acoustic Microscopy and Diagnostic Ultrasound, *Ultrasound Imaging*.

*Weglein, R. D., and Wilson, R. G., The Scanning Acoustic Microscope — A New Diagnostic Tool for Integrated Circuits and Materials, *Proc. Adv. Tech. in Failure Analysis Symp.*, Los Angeles, California, November 6-9, 1978.

*Wilson, R. G., and Comas, J. Correlation of Atomic Distribution and Implantation Induced Damage Profiles in Be Ion-Implanted Silicon, *Radiat. Eff.*

*Wilson, R. G., and Comas, J., Channeling

*Reports of Contract Research.

(Continued on Back Cover)

NBS-114A (REV. 9-78)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBSIR 79-1591	3. Recipient's Accession No.

4. TITLE AND SUBTITLE

Semiconductor Technology Program - Progress Briefs

5. Publication Date

January 1979

7. AUTHOR(S)

W. Murray Bullis, Editor

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, DC 20234
and various contractor facilities (as noted)

11. Contract/Grant No.

See item 15

12. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS *(Street, City, State, ZIP)*

NBS, Washington, DC 20234; ARPA, Arlington, VA 22209; DNA, Washington, DC 20305; Dept. of Energy, Washington, DC 20545; C. S. Draper Laboratory, Cambridge, MA 02139; AFAL, Wright-Patterson AFB, OH 45433; Army Electronics R&D Command, Ft. Belvoir, VA 22260; NavMat Command, Hdqtrs., Washington, DC 20360; NWSC, Crane, IN 47522.

13. Type of Report & Period Covered

Interim
July - Sept. 1978

15. SUPPLEMENTARY NOTES

ARPA Order 2397, Program Code 8Y10; DNA IACRO 78-807; Dept. of Energy, Interagency Agreement EX-77-A01-6010, Task Orders A021-EES and A054-SE; C. S. Draper Laboratory, P. O. DL-H-139485 (Navy contract N 00030-78-C-0100); AFAL, MIPR FY117578N2026; Army Electronics, MERADCOM, P. O. 28052; NavMat Command, N0003778IP89010; NWSC, N0016478WR30055.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include studies of: laser annealing of low-fluence implants in silicon; analysis techniques for spreading resistance profiling measurements; Hall effect measurements in two-layer structures; incorporation of hydrogen and hydroxyl impurities in silicon dioxide films; an integrated gated-diode electrometer test structure; defect-density profiling by constant-capacitance deep-level transient spectroscopy; and a spatial integrity test pattern for electrical measurement of intra- and inter-die line-width variations. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

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- [x] Order From National Technical Information Service (NTIS), Springfield, VA. 22161

19. SECURITY CLASS (THIS REPORT)	21. NO. OF PRINTED PAGES
UNCLASSIFIED	12
20. SECURITY CLASS (THIS PAGE)	**22. Price**
UNCLASSIFIED	$4.00

USCOMM-DC

(Continued from Page 12)

and Random Equivalent Depth Distributions of 150-keV $^{7}_{3}Li$, $^{9}_{4}Be$, and $^{11}_{5}B$ Implanted into <100> and <110> Silicon, *Radiat. Eff.*

*Wilson, R. G., Dunlap, H. L., Jamba, D. M., and Myers, D. R., *Semiconductor Measurement Technology:* Angular Sensitivity of Controlled Implanted Doping Profiles, NBS Spec. Publ. 400-49.

*Wilson, R. G., and Weglein, R. D., Acoustic Material Signatures Using the Reflection Acoustic Microscope, *Proc. 1st Internat. Symp. Ultrasonics Matls. Characterization,* Washington, D.C., June 8-10, 1978.

*Reports of Contract Research.

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