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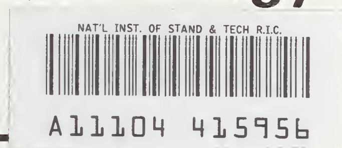
Semiconductor Technology Program Progress Briefs



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SEMICONDUCTOR TECHNOLOGY PROGRAM

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ABSTRACT — This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include studies of: process-induced radiation damage; resistivity-dopant density relationships in silicon; spreading resistance measurements; spreading resistance profiling; cross-bridge sheet resistor test structure; PIND test; and moisture infusion into hermetic packages and conduct of a workshop on power semiconductor devices. In addition, brief descriptions of new and selected ongoing projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

KEY WORDS: Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

This report covers results of work during the forty-second quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Solar Energy Research Institute; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 7. The Army Electronics R&D Command; 8. The Air Force Avionics Laboratory; 9. The Naval Material Command; and 10. The Naval Weapons Support Center.

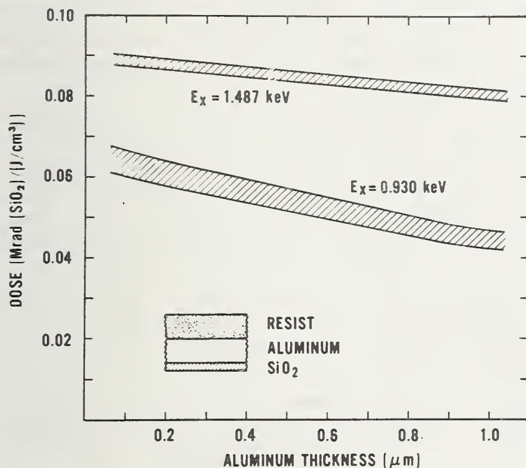
This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

Process-Induced Radiation Damage

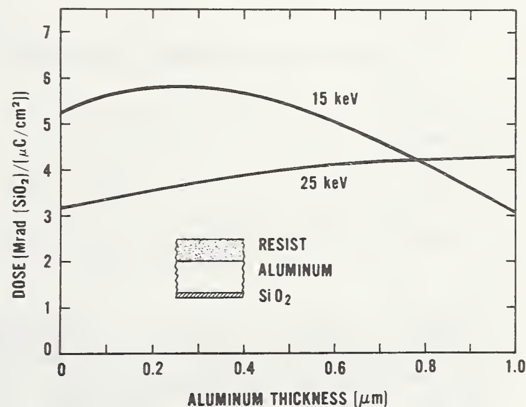
Additional calculations have been made of the radiation absorbed dose incurred by oxide layers during exposure of positive resist films during x-ray or direct-write electron-beam lithography. In order to make an explicit calculation, a typical device-like structure consisting of a silicon dioxide layer, 50 nm thick, under an aluminum layer from 100 to 1000 nm thick under a resist layer was assumed. In the case of x-ray lithography, the calculations were made for both aluminum (1.487 keV) and copper (0.930 keV) characteristic x-rays impinging on a resist layer 500 to 1000 nm thick. In the case of electron-beam lithography, the calculations were made for both 15- and 25-keV electrons impinging on a resist layer 500 nm thick. The results of the calculations are presented in the accompanying figures as absorbed dose per unit exposure dose or incident flux as a function of aluminum thickness. Exposures required for typical x-ray resists range from about 1 to about 500 J/cm^3; thus, the radiation absorbed dose during x-ray lithography may range from 0.04 to 50 Mrad (SiO_2). Fluences required for typical electron-beam resists range from about 0.05 to about 50 $\mu C/cm^2$; thus, the radiation absorbed dose during electron-beam lithography may range from about 0.15 to 300 Mrad (SiO_2). [Sponsors: 1,2,]

(K. F. Galloway, S. Mayo, and P. Roitman,* x3625)

*NBS-NRC Postdoctoral Research Associate.



Radiation absorbed dose in a 50-nm thick silicon dioxide layer of a typical resist-coated MOS structure for an x-ray exposure of 1 J/cm^3, plotted as a function of the thickness of the aluminum metallization. Results are shown for characteristic x-rays from aluminum (1.487 keV) and copper (0.930 keV). The band width indicates a variation in resist thickness from 500 nm (at the top of the band) to 1000 nm (at the bottom of the band).



Radiation absorbed dose in a 50-nm thick silicon dioxide layer of a typical MOS structure coated with 500 nm of resist for an incident electron beam fluence of 1 $\mu C/cm^2$, plotted as a function of the thickness of the aluminum metallization. Results are shown for electron beam energies of 15 and 25 keV.

Resistivity-Dopant Density Evaluation

Empirical expressions were developed to fit resistivity-dopant density data measured on phosphorus-doped silicon with resistivity, ρ, in the range from 0.00085 to 160 $\Omega\cdot$cm (dopant density, N, in the range from 9×10^{19} to 2.7×10^{13} cm^{-3}). A nonlinear least squares method using the DATAPLOT language was employed in the fitting procedure. The expressions are in the form of quotients of two third degree polynomials of the form:

$$\log F = \frac{A_0 + A_1X + A_2X^2 + A_3X^3}{1 + B_1X + B_2X^2 + B_3X^3} .$$

The function F is the product $q\rho N$ (where q is the electronic charge) normalized to 1 $C\cdot\Omega/cm^2$ ($V\cdot s/cm^2$); fits were obtained for both $X = \log(\rho/\rho_0)$ and $X = \log(N/N_0)$ with $\rho_0 = 1\ \Omega\cdot$cm and $N_0 = 10^{16}\ cm^{-3}$ for temperatures of 23°C and 300 K. These normalization factors were selected so that $|X| < 4$ over the entire range.

Coefficients for the Fits of Resistivity-Dopant Density Data at 23°C.

F	$q\rho N/(q\rho N)_0$		μ_e/μ_{e0}	
X	$\log(\rho/\rho_0)$	$\log(N/N_0)$	$\log(\rho/\rho_0)$	$\log(n/n_0)$
A_0	-3.1112	-3.0770	3.1104	3.0774
A_1	-3.3650	2.3113	3.3501	-2.3506
A_2	-1.2914	-0.66228	1.2738	0.67827
A_3	-0.16110	0.066679	0.15906	-0.067513
B_1	1.0558	-0.71242	1.0513	-0.72698
B_2	0.40896	0.20928	0.40266	0.21413
B_3	0.050481	-0.022091	0.050027	-0.022021

Normalization factors:

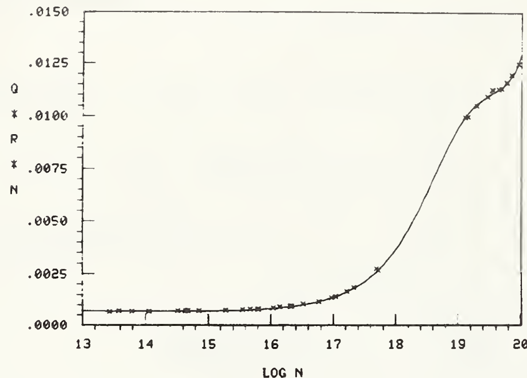
$(q\rho N)_0 = 1\ V\cdot s/cm^2$

$\mu_{e0} = 1\ cm^2/V\cdot s$

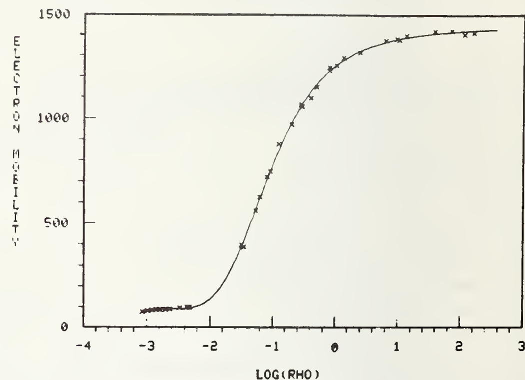
$\rho_0 = 1\ \Omega\cdot cm$

$N_0 = n_0 = 10^{16}\ cm^{-3}$

Fits were also obtained for electron mobility, μ_e, but it was necessary to convert the dopant density to electron density, n, before making the computation; the published results of Li and Thurber were used for this conversion. In this case the function F is the elec-



Computer-generated plot of the product of electronic charge (Q) in coulombs, resistivity (R) in ohm-centimeters, and dopant density (N) in reciprocal cubic centimeters as a function of log N for phosphorus-doped silicon at a temperature of 300 K. Experimental data are shown as crosses. In computing the fit, shown as a solid curve, 16 was subtracted from log N as discussed in the text.



Computer-generated plot of the electron mobility in square centimeters per volt-second as a function of the log of resistivity (RHO) in ohm-centimeters for phosphorus-doped silicon at a temperature of 300 K. Experimental data are shown as crosses; in computing the electron mobility, dopant density was converted to carrier density as discussed in the text. The computer fit is shown as a solid curve.

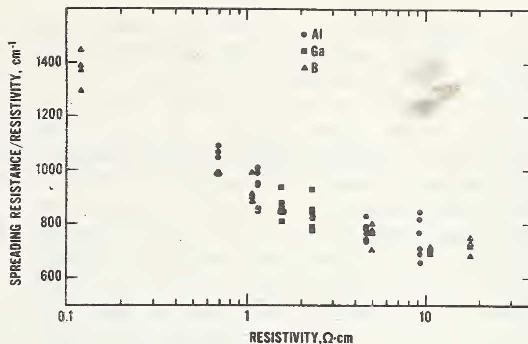
tron mobility normalized to 1 $cm^2/V \cdot s$ and X equals log (ρ/ρ_0) or log (n/n_0) with $n_0 = 10^{16}$ cm^{-3}. Again, fits were obtained for temperatures of 23°C and 300 K.

The coefficients for the 23°C cases are listed in the accompanying table. Although each expression contains seven coefficients, the computation is straightforward and results in smooth curves as illustrated by the accompanying plots of $q\rho N$ *vs.* N and μ_e *vs.* ρ, both for a temperature of 300 K. [Sponsors: 1,2] (W. R. Thurber, x3625, R. L. Mattis and Y. M. Liu, x3541, and J. J. Filliben, x3651)

Spreading Resistance Measurements

Studies of the effect of specimen surface preparation on measurement of the spreading resistance of high-resistivity (111) *n*-type silicon were completed. In addition, more extensive tests were made to compare the effects of specimen preparation on the spreading resistance calibration response for both *p*- and *n*-type specimens over the entire resistivity range appropriate to thyristor fabrication. The results confirmed earlier indications that, overall, polishing with 0.5-μm diamond grit in a nonaqueous medium against a nonwoven polishing cloth yielded the most satisfactory surface conditions. Compared with measurements on specimen surfaces polished in the customary way with colloidal silica, measurements on specimens with 0.5-μm diamond-polished surfaces showed (1) comparable signal-to-noise level throughout the resistivity spectrum, (2) nearly the same overall response for the entire resistivity range of *p*-type specimens and for the *n*-type specimens below 1 Ω·cm, and (3) both more reproducible and more linear (with resistivity) results for *n*-type specimens with resistivity greater than 1 Ω·cm.

A test was conducted to verify the applicability of spreading resistance calibration data obtained on boron-doped



Spreading resistance response for boron-, gallium-, and aluminum-doped silicon.

silicon to analysis of aluminum- or gallium-doped specimens. Spreading resistance measurements were made on boron-, gallium-, and aluminum-doped silicon in the resistivity range commonly used for thyristor fabrication. As shown in the accompanying figure, no effect due to dopant species could be determined within the error limits imposed by the basic repeatability of the measurement and the resistivity uniformity of the test specimens. [Sponsor: 3] (J. R. Ehrstein, x3625)

Spreading Resistance Profiling

Shallow-angle beveling for depth profiling by spreading resistance imposes a requirement for very flat surfaces that is not imposed for measurements on top surfaces of specimens. Use of diamond polishing was tested for applicability to preparing beveled specimens for depth profiling by spreading resistance measurements. To avoid edge rounding at the intersection of the bevel and the top surface, it is necessary to polish the specimen against a hard work surface. Polishing with 0.1-μm polycrystalline synthetic diamond grit in a nonaqueous medium on a glass plate which had been previously frosted using 9-μm aluminum oxide was found to be a satisfactory procedure. The beveled silicon surface so obtained has a somewhat higher scratch density than that which

was obtained when polishing large area top surfaces with 0.5-μm diamond grit against a nonwoven polishing cloth. However, this scratch density does not seem to affect the quality of spreading resistance depth profiles. Further, surface profilometer measurements indicated that even very shallow angles as small as 6 min of arc had sharp intersections with the top surface. Such sharp bevels allow more accurate profiles to be made than can be made on bevels prepared by polishing with colloidal silica which typically display a rounded region near the intersection. To bevel actual thyristor structures, larger bevel angles (3 to 10 deg) must be used. Because the 0.1-μm diamond is too fine to remove the required amount of material in a reasonable time, a multiple-step process with several different grades of grit must be used. This process is generally satisfactory, although particular care is required to avoid degradation of surface quality which may adversely affect the data. [Sponsor: 3] (J. R. Ehrstein, x3625)

Cross-Bridge Sheet Resistor

Initial studies of the sensitivity of the cross-bridge sheet resistor test structure to geometric variations were carried out. This test structure is intended for measurement of sheet resistance and linewidth of diffused, implanted, or metal regions. This phase of the work involved investigation of geometrical effects on the measured value of the linewidth. Geometrical properties studied included the width of the voltage taps in the bridge portion of the structure and the distances between the two taps and between a tap and the nearest current contact corner. Results suggest that the current penetration into the taps is substantially less than previously estimated and that errors in measured linewidth are less than 1% for taps the same width as the line being measured, spaced 20 linewidths apart. This geometry is frequently found in cross-bridge structures. Narrower taps, of course, introduce even less error; rounding of the corners where the tap meets the line (which becomes significant for taps and lines less than 5 μm wide) tends to increase the error somewhat. The taps can be placed as close as one linewidth to a current contact corner without introducing a measurement error as great as 0.5%. [Sponsor: 1]
(R. L. Mattis, x3541)

PIND Test Evaluation*

Evaluation studies of the particle impact noise detection (PIND) test for screening microelectronic devices for the presence of loose particles were completed. Procedures and apparatus specified in Test Method 2020 of MIL-STD-883, Test Methods for Electronics, were compared. For the major experimental effort, specially prepared test packages were used. Particles of a variety of shapes, sizes, and materials characteristic of those likely to be found in devices as a result of processing steps were used to seed most of these packages; some packages were left unseeded as controls. One of the principal problems with the PIND test is the immobilization (lock-up) and release of particles through electrostatic and other mechanisms. The present series of experiments showed evidence of uncontrolled lock-up of particles in seeded packages; flatpacks or DIPs with ceramic parts showed a greater tendency to such lock-up than did metal cans. Despite the uncertainties introduced by the lock-up problem, the following recommendations were made: (1) that semiautomatic apparatus, with preset detectability levels, be used to avoid effects due to operator variability; (2) that parametric trials be conducted on each package type to be tested in order to determine appropriate test conditions and de-

*Work carried out in the NBS Electrosystems Division under the sponsorship of the NASA Goddard Space Flight Center (Purchase Order S39193-B). Although this work was conducted independently from the Semiconductor Technology Program, the results are included here because of the widespread interest of the semiconductor electronics community in this test.

tectability levels; (3) that consideration be given to limiting the initial acceleration levels to $\pm 10\ g_n$ for some package types; (4) that the maximum permitted output impedance of the detection transducer assembly be specified to avoid cable noise problems; and (5) means be developed to avoid exceeding the specified preshock acceleration levels (as did the acceleration level provided by the commercial preshock apparatus, one allowed by Test Method 2020, used in the tests) in order to minimize damage to the devices. A complete report of the work has been published as NBSIR 78-1590 (NASA), Loose-Particle Detection in Microelectronic Devices.

(J. S. Hilten, P. S. Lederer, J. F. Mayo-Wells, and C. F. Vezzetti, x3821)

Moisture Infusion Into IC Packages

A preliminary study of the relationships between moisture infusion, leak size, and device reliability has been completed at Martin Marietta Aerospace. Two sets of experiments were conducted. In one, packages constructed with a controlled leak and an oxide-type moisture sensor were placed in a controlled humidity environment and the water vapor content measured as a function of time. The packages tested had leak sizes in the range between 10^{-9} and 10^{-5} atm·cm^3/s. The second experiment was a 5000-h life test in which 186 packages, each of which contained unpassivated 741 operational amplifier chips, were subjected to an atmosphere with 85% relative humidity at 85°C. In this case the packages had measured leak sizes between 10^{-9} and 10^{-3} atm·cm^3/s. The results exhibited a great amount of scatter, both because of the primitive nature of the measurement methods available for use in this type of experiment and because of the large variability in both water vapor infusion and the reactions of water vapor on device surfaces. Nevertheless, it can be safely concluded that present leak rate limits for large packages are not low enough to insure that the maximum permissible moisture level will not be exceeded during a reasonable service life. [Sponsor: 1]

(S. Ruthberg,* x3621)

Power Devices Workshop

A Workshop on Power Semiconductor Devices, cosponsored by the IEEE Electron Devices Society and NBS, was held at NBS/Gaithersburg on December 7, 1978. This was the first workshop to bring together technical experts to discuss freely the status of technical problems that impede progress in the field of power semiconductor devices. The workshop was attended by 86 scientists and engineers; 22 participants were from outside the U.S. Following brief formal presentations, four working groups were formed to deal with the following topics: transistor reverse-bias safe operating area considerations, thyristor modeling, transistor modeling, and high-voltage junction technology. At the conclusion of the program, all attendees had an opportunity to hear and discuss the findings of the individual working groups. The participants at this plenary session agreed that the workshop had been valuable and that the activity should be regarded as a continuing one. Plans are already underway for a second workshop next year. A summary of the results of the workshop will be included in a future issue of the Electron Devices Society Newsletter. [Sponsor: 2]

(F. F. Oettinger, x3621)

Future Event . . .

A Workshop on Photovoltaic Material and Device Measurements will be held in Arlington, Virginia, on June 11 to 13, 1979. The workshop, sponsored by the Solar Energy Research Institute in association with NBS, is intended to accelerate the development of thin film solar cells by improving the versatility and reliability of material and device measurement techniques. The workshop will be restricted to polycrystalline materi-

*NBS Contact.

als and devices; amorphous material and devices will not be discussed. Sessions are planned in measurements for structural and chemical properties, optical and electro-optical properties, and charge transport properties. The workshop will be cochaired by D. E. Sawyer (NBS) and J. Morabito (Bell Laboratories). [Sponsor: 4]
(D. E. Sawyer, x3621)

New Topics . . .

Thermal Resistance Standards — A new project was begun to enable NBS to supply standard reference materials (SRMs) for thermal resistance to the semiconductor device industry. The SRMs will be in the form of selected commercially available power transistors that have been characterized and certified as to their thermal resistance properties. The initial group of SRMs, expected to be completed early in 1980, will be comprised of transistors in TO-3 packages. Dedicated equipment to perform the measurements is now being designed and constructed. [Sponsor: 2] (D. L. Blackburn and D. W. Berning, x3621)

Linewidth Standards — An automated scanning photometric optical microscope system is being assembled for use in measuring photomask-like linewidth calibration artifacts. These artifacts are being developed as standard reference materials for measurements on chrome photomasks with transmitted light. The artifacts themselves will be similar to the ones being employed in the interlaboratory evaluation of NBS-developed linewidth measurement procedures; modifications based on the findings of the evaluation are planned to facilitate use of the artifacts. [Sponsor: 1]
(J. M. Jerke and D. Nyyssonen, x3621)

Update . . .

A final report covering the development, at RCA Laboratories, of apparatus and procedures for extended range MIS C(V) measurements has been published as NBS-GCR-78-155. This report provides a complete summary and cross index of the various publications which have appeared as a result of this work, together with an errata section which includes several revised circuit diagrams, the prior versions of which contained minor errors or omissions. Since use of the corrected diagrams and other items will facilitate construction of the apparatus, persons planning to replicate this measuring system should be sure to obtain a copy of the final report. [Sponsor: 1]
(R. Y. Koyama,* x3625)

Work in Progress . . .

Isothermal Transient Capacitance (ITCAP) techniques were utilized to characterize platinum defect centers introduced into 3 to 5 Ω·cm (111) *n*- and *p*-type silicon. Following processing of the wafers with test pattern NBS-3, the platinum was introduced by diffusion from a spin-on platinum-silica emulsion applied to the back surface of the wafer. The diffusions were carried out in flowing nitrogen for 1 h at 900°C for the *n*-type wafer and at 1000°C for the *p*-type wafer, resulting in platinum densities of about 5 to 7 × 10^{14} cm^{-3}. ITCAP measurements were made on the gated diode test structure (3.10). An electron trapping center 195.5 ± 2 meV below the conduction band edge was observed in the *n*-type wafer, and a hole trapping center 289 ± 2 meV above the valence band edge was observed in the *p*-type wafer. Emission coefficients were observed to be 1.43 × 10^6 (±26%) and 3.33 × 10^6 (±18%) $s^{-1} \cdot K^{-2}$, respectively. Many energy levels associated with platinum have been reported in the literature. The specific origins and nature of each of these centers have not yet been established. [Sponsor: 2,3]
(W. E. Phillips and R. Y. Koyama, x3625)

*NBS Contact; the assistance of J. L. Repace at the Naval Research Laboratory in identifying errors in the published reports is gratefully acknowledged.

A closed form expression has been derived for the decay of the open-circuit voltage of a gated diode for the case where the gate voltage is such as to accumulate the underlying silicon. It is found that the voltage does not have a simple exponential dependence on time but that the generation lifetime in the depletion region beneath the junction can be found from the initial slope of a plot of log voltage against time. In inversion, the initial slope of this plot yields an effective lifetime, which includes contributions from the depletion regions both beneath the junction and beneath the gate. [Sponsor: 1]
(M. G. Buehler, x3541)

Analysis of the data received to date in the interlaboratory evaluation of the procedures for measuring linewidths in the 1- to 10-μm range on chrome photomasks using transmitted light is in progress. Preliminary results suggest both that significant data spreads (0.3 to 0.6 μm) may occur within individual organizations and that differences between values measured by NBS and the industrial participants are not always largest for the smallest (0.5- to 0.9-μm wide) lines where optical resolution of the measuring equipment would be expected to be the limiting factor. [Sponsor: 1] (J. M. Jerke, x3621)

The laser scanner has been modified so that solar cells up to 100 mm in diameter may be scanned without repositioning. The diameter of the scanning probe beam is 25 μm. Cells of different types being developed by a number of SERI subcontractors have been scanned to search for possible defects and reveal details of cell operation. Of particular interest at the present time are passivated and unpassivated polycrystalline silicon cells. [Sponsor: 4]
(D. E. Sawyer, x3621)

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include studies of: process-induced radiation damage; resistivity-dopant density relationships in silicon; spreading resistance measurements; spreading resistance profiling; cross-bridge sheet resistor test structure; PIND test; and moisture infusion into hermetic packages and conduct of a workshop on power semiconductor devices. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

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