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Beyond Silicon: Novel Materials Heterostructures for Future High-Performance Computing

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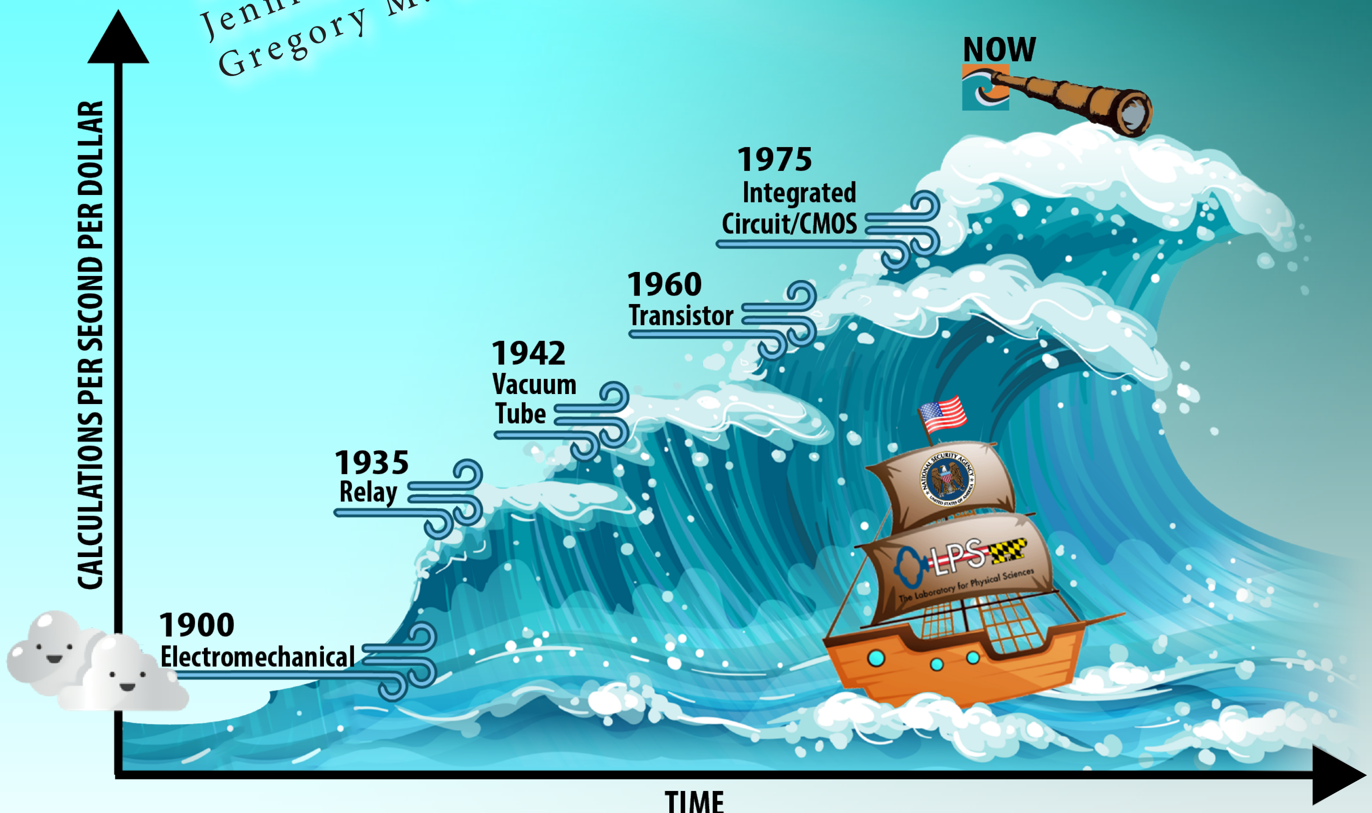


For the last 75 years, the operation of the majority of electronics has been based on manipulating electron charge in the elemental semiconductor silicon. The basic device operation of the silicon transistor is referred to as complementary metal-oxide-semiconductor (CMOS). While this paradigm was amazingly successful for generations, CMOS is reaching its physical limits and will be unable to keep pace with the speed, energy, and size requirements critical for data manipulation and the storage needs of the commercial, defense, and intelligence communities. Research into the next generation of materials and devices is therefore essential to enable future high-performance computing (HPC) platforms.

Consider that technologies are like waves (as in figure 1)—they slowly build up and then eventually crest while a new wave builds—a suitable analogy for this publication. Moore's law, the empirical observation that the number of transistors on a chip doubles approximately every two years, is the de facto driving force behind the current wave and has resulted in exponential growth in computing power. Troublingly, no new wave has been clearly identified. Without a firm path beyond the current paradigm—the Next Wave—critical computing needs will not be met.

Background

To enable future HPC systems, we need to imagine and create innovative solutions to fuel the next wave. This includes developing devices that incorporate alternate-state variables, for example, electron spin (i.e., spintronics), magnetism, or photonic devices that utilize inherent material properties besides electron charge to manipulate information. Ultimately, a "materials-by-design" solution will be feasible by combining different materials to create the necessary properties. Beyond the development of new devices, the entire advanced computing system problem space—material, device, architecture, etc.— must be holistically considered, a concept referred to as codesign.

FIGURE 1. The waves of technology from 1900 to now are much like waves in an ocean. A new wave increases the total calculations per second per dollar with each new technology. The wave builds up slowly, then quickly gains momentum and takes over, finally cresting while a new wave begins building. There is no clear next wave on the horizon. Technology users ride the waves like boats in the ocean. Researchers work to identify new waves before the prior waves crash onto them.

Research into alternate-state variables, coupled with breakthroughs in materials science that include entirely new materials classes with a host of advantageous properties, is generating a considerable amount of excitement in the HPC field for novel materials and devices. In particular, devices fabricated from novel two-dimensional (2D) materials, topological Dirac materials, or novel magnetic materials are expected to offer an avenue for lower-power, higher-performance memory and logic beyond Moore's law [1, 2]. However, basic research must be performed to identify the best materials and alternate-state variables to use from the available new classes. In addition, we must better understand how to make usable devices with combinations of these materials that optimize properties and solutions.

The Laboratory for Physical Sciences (LPS) has a novel materials and devices research program, and our objective in this program is to explore the properties of devices that incorporate emerging materials such as topological Dirac materials, 2D materials, and magnetic-phase-change materials with a goal of creating better capabilities (e.g., faster speed, lower-power, greater versatility/functionality) for memory, logic, and HPC beyond the paradigms established by Moore's law. This requires high-risk, high-reward research that is focused on understanding the unknown basic properties of promising new materials, determining exactly which properties can be exploited to the greatest effect, and designing, fabricating, and

testing devices that use these properties and that can be quickly transitioned into technologies with the potential for disruptive, non-incremental discovery and implementation. In this article, we will briefly discuss two recent prototype devices developed at LPS: topologically enabled spintronic devices further exemplified by a cadmium arsenide (Cd_3As_2)/fluorographene heterostructure non-local spin valve, and a metamagnetic iron rhodium (FeRh) memory element.

Topologically enabled electronics

Topological materials have special properties enabled by their physical structure, or topology. Topological Dirac materials, a recently discovered class of materials, have the potential to enable spintronics as the defining technology of future electronic systems [3]. In these materials, the conduction and valence energy bands meet at a single "Dirac point," resulting in a host of exciting properties such as relativistic electronic transport and dissipationless spin transport.

The most well-known Dirac material is graphene, a 2D version of graphite. Another is bismuth selenide (Bi_2Se_3), a so-called topological insulator because only its surface conducts electricity [4]. Another promising new material is Cd_3As_2, which is a topological Dirac semimetal (TDS). This material can be tuned between multiple quantum phases (QPs), allowing for a truly multifunctional material [5]. While CMOS relies on toggling between charge states, a system made with Cd_3As_2 devices could reversibly switch between computing modes by toggling between the QPs—a process that is both faster and lower energy, while at the same time allowing inherent reprogrammability and multifunctionality.

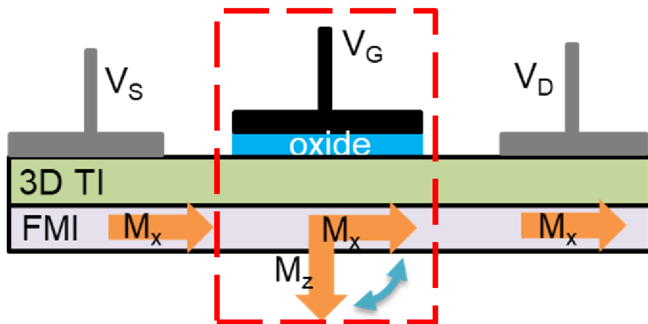
In a recent, exciting agency first, LPS received funding support from the Office of the Under Secretary of Defense, Research & Engineering as part of an Applied Research for the Advancement of Science and Technology Priorities (ARAP) program in collaboration with the Army Research Laboratory, Naval Research Laboratory, and the Air Force Research Laboratory. The purpose of the program is to design, fabricate, and prototype new Dirac material/topological memory and logic devices with technologically disruptive potential. Two identified pathways are through topological magnetoelectronic (TMET) logic and with magnetic topological memory (MTM).

The TMET project is concentrated on a device that works by using an external electric field to toggle the direction of a magnetic field in close proximity to a topological Dirac material, thereby using the magnetic interaction to switch a transistor-like device ON or OFF. This quantum transistor would operate at 1,000 times less power and 10 to 1,000 times faster speeds than today's state of the art. The MTM device operates by exploiting a unique property of a topological Dirac material—its spin is locked to its momentum. Using a process called spin-orbit-torque (SOT) to change the magnetic moment of an element, called a magnetic tunnel junction (MTJ), it provides the same functionality as commercial magnetoresistive random-access memory (MRAM). However, SOT-MTJs are significantly faster and use a fraction of the energy compared to commercial MRAM. The charts in figure 2 summarize the ARAP technologies.

For topologically enabled devices to become reality, we first must better understand the fundamental behavior of the materials. For example, how long does it take spins to scatter? How efficient is the spin-charge conversion? Recently, LPS was one of the first to answer these questions by investigating the spin Hall effect (SHE) in topological Dirac materials using a method previously used to investigate atomically heavy metallic materials. The SHE occurs when a charge current passes through a material with a high spin-orbit coupling (like a topological material), which functionally acts as an internal magnetic field, thereby producing a perpendicular spin current. The effect is reversable: a spin current also produces an orthogonal charge current via the inverse spin Hall effect (ISHE).

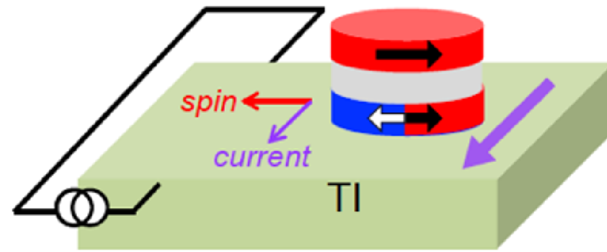
Thus, the SHE and ISHE directly measure how efficiently a material converts charge currents into spin currents and vice versa. In addition, these measurements can also tell us the spin diffusion length and spin relaxation time, which are measures of how far the spin travels before it scatters and how much time elapses between scattering events. A more robust spin current will directly lead to more robust information manipulation in future devices.

(a) Topological Logic



PROPERTY	HIGH-PERFORMANCE CMOS	TMET
Subthreshold slope	Typical: 70mV/dec Theoretical min @ RT: 60mV/dec	0.7–40mV/dec (Value limited by magnetism, not temp)
Operational power loss per 32-bit ALU	0.1 mW	1 μW
Device optimization	Reaching limits of engineering (e.g., FinFet, Chiplet)	New parameter space to optimize Structural device optimizations are transferable (e.g., FinFet)
High-frequency response	Requires complex HEMT material stacks	Naturally high-mobility channels

(b) Topological Memory



PROPERTY	CMOS NVM (E.G., FLASH, STT MRAM)	TOPOLOGICAL MRAM
Bit-switch energy cost	10^{-9} J	10^{-18} –10^{-15} J
Switching speed (RAM is > 1 GHz)	100–1000 MHz Only USB storage	1–10 GHz Ferromagnet 1 THz antiferromagnet Operable as RAM
Power dissipation if used as RAM	0.1–1 W/bit	10–10^4 nW/bit
Industrial maturity	End of Moore. Seventy years of advancements nearing end.	Non-topological MRAM Shipped in 2016 (Everspin) (Everspin, 1 Gb, 2019)

FIGURE 2. (a) In this schematic of the topological magnetoelectronic transistor (TMET) device, a 3D topological insulator Dirac material (3D TI) sits on a ferromagnetic insulator (FMI) with a magnetic moment that toggled using an oxide gate (red dotted line). The device toggled on/off by switching the direction of the magnetic moment in the FMI. The advantages are indicated in the chart by color: red fails to meet future requirements, yellow barely meets future requirements, and green fully meets future requirements. **(b)** In this schematic of the magnetic topological memory device, a charge current in a topological Dirac material is naturally transduced into a spin current. The spin current interacts with a magnet that is a layer in a magnetic tunnel junction (MTJ). MTJs are created by sandwiching an insulating material between two ferromagnetic materials. When the magnetic moments of the two ferromagnets are parallel/antiparallel, the resistance is low/high. The resistance state is written or read depending on the applied current. The advantages are indicated in the chart by color.

The SHE and ISHE measurements are performed as shown in figure 3. This geometry, called a Hall bar, is the basis for a wide variety of electronic measurements. When a conventional charge current passes between one set of side contacts (left), it produces a spin current in the central channel via the SHE. When this subsequent spin current reaches a second set of contacts (right), the spin current converts back into a charge current via the ISHE. Because the circuit does not directly connect these two sets of contacts, the resulting charge current in the contacts on the right manifests as a voltage. By applying a magnetic field along the initial charge current path, we can disrupt the flow of spins and measure the resulting effect on the voltage. The applied field causes the spins to precess, or rotate around an axis, reducing the measured voltage as a decaying oscillatory function of the applied field [6]. The voltage decrease is directly proportional to the spin-charge conversion efficiency of the material, and its decay gives us the spin diffusion length and spin relaxation time.

Metals like platinum (Pt) and tungsten (W) are currently used in spin-orbit torque-based MRAM designs and have spin-charge conversion efficiencies on the order of 0.05-0.1. The efficiency for topological materials can be more than 10 times larger. The topological insulator bismuth antimony ($Bi_{0.9}Sb_{0.1}$) has an efficiency as high as 52 [7].The efficiency is directly proportional to the current required to switch a bit: 10 times higher spin efficiency will result in 10 times less needed current and therefore 10 times less power. The spin diffusion length and relaxation time gives limits on the speed and dimensions of the devices, as any manipulation of the spins must occur before the spin information disappears. Based on these measurements, we can begin to select materials that optimize our device designs.

Cd_3As_2/Graphene spin valves: A novel topological Dirac material/2D heterostructure

Cd_3As_2 is an excellent candidate for topologically enabled electronics. Cd_3As_2 has a tunable quantum phase, a high mobility, microns-long spin diffusion lengths, and high spin-charge conversion efficiency. We have also identified a 2D material, fluorographene, as an excellent material to use to couple to the Cd_3As_2 to build a spintronic heterostructure. We want to combine these materials because when disparate materials (e.g., Dirac materials, 2D materials, and novel magnetic materials) form heterostructures, the individual properties of each material can overlap due to atomic-level proximity. As an example of how powerful this

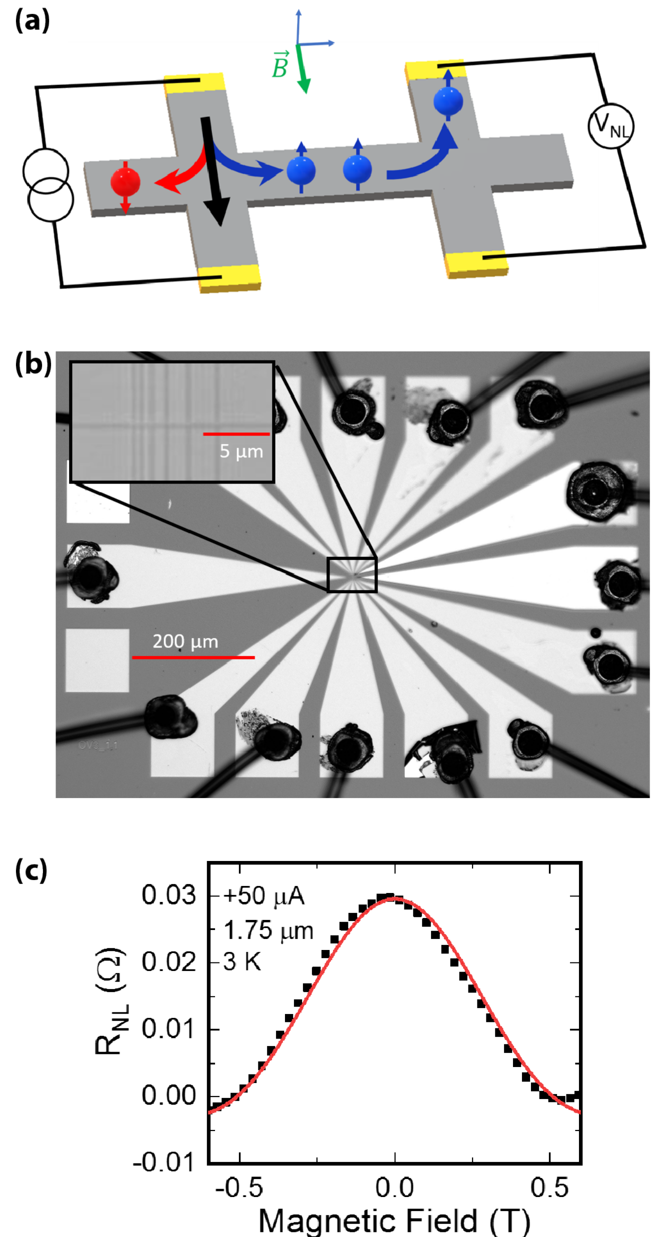


FIGURE 3. (a) This schematic of a spin Hall effect (SHE) device shows a charge current flowing through the contacts on the left, which generates a spin current. When the spin current reaches a second set of contacts outside of the charge current path (on the right of the schematic), it creates a measurable voltage. **(b)** This optical image is of a topological SHE device. (R_{NL} stands for non-local resistance.) **(c)** When a magnetic field is applied in plane, the spins begin to precess. Sweeping the field causes dephasing (black dotted curve). The data are fit to a model (red line) and important parameters can be extracted.

technique can be, consider a stack of 2D materials. These are single layer sheets ranging from one to five atoms thick, are mechanically flexible, can be grown in large areas, and can have various electronic states (e.g., semiconductor, metal, semimetal, superconductor, insulator, etc.). They are discretely stackable so they can be used to create true materials by design, where the final bulk heterostructure contains material properties made to order [8]. Two layers of graphene, atomically thin layers of carbon atoms, can be stacked on top of each other and, depending on the relative angle between them, can be insulating, metallic, or even superconducting.

The fundamental spintronic device is the nonlocal spin valve (NLSV). Here, spin current in a channel is compared to a magnet moment in a detector contact. Depending on the relative orientation of the contact with the injected spin moment, there will be a high- or low-magnitude resistance in the device. Figure 4 shows an optical image of a NLSV along with a schematic representation. Two tunneling ferromagnetic contacts (center lines, fluorographene/magnesium oxide (MgO)/Permalloy (Py) are placed on top of a spin-transport channel, in this case Cd_3As_2[9]. Py is a magnetic alloy containing 80 percent nickel and 20 percent iron.

The spintronic behavior of the NLSV is entirely enabled by the fluorographene/MgO tunnel barrier. Electronic tunneling is a quantum mechanical effect occurring when electrons "tunnel" or pass through materials that classically should block them. As an analogy, one can think of a ball thrown at a brick wall. Classically, the ball will bounce back. However, quantum mechanically, the ball will occasionally go through and come out on the other side. For the NLSVs, this barrier is essential due to the electronic properties of the ferromagnet (FM) and the spin channel. The FM is a normal metal, but the spin channel is a semimetal; it conducts current but far less efficiently than the FM. Without the tunnel barrier, the spin channel could not handle the number of electrons trying to move through it, so they bounce off the interface and interfere with the ones that do get through. The tunnel barrier acts as a sort of flow regulator, limiting the number of electrons that get through and allowing for a much smoother flow of electrons into the device.

Graphene makes an excellent tunnel barrier due to its 2D nature. Graphene is conductive in-plane, but highly resistive out-of-plane. It can be discretely stacked (at 0.3 nanometers thick!) onto any surface, is self-healing, is pinhole free, and can further serve

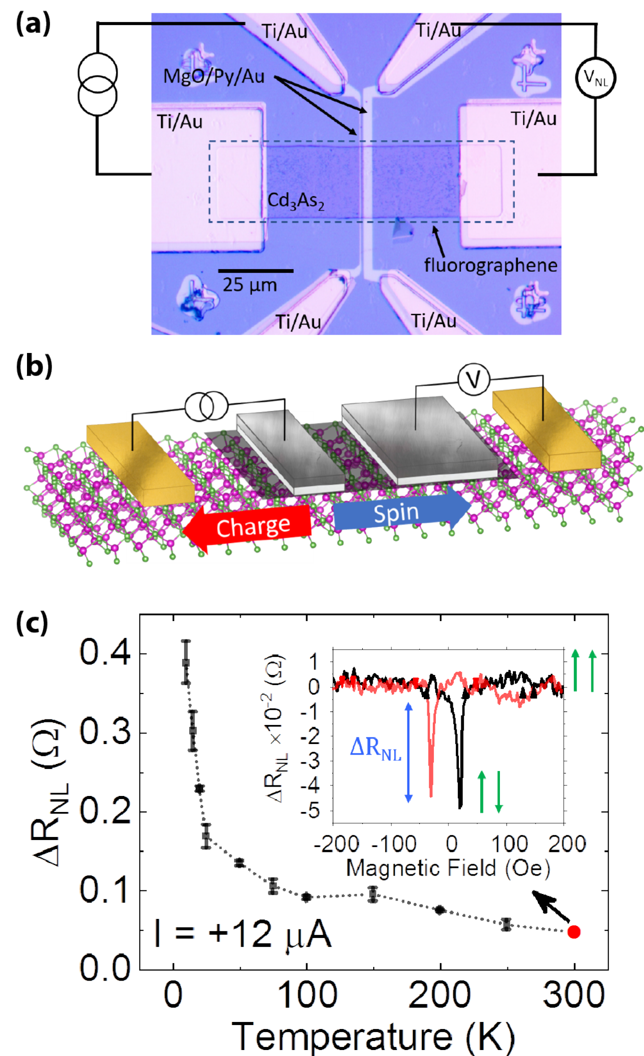


FIGURE 4. (a) In this optical image of a Cd_3As_2/fluorographene non-local spin valve, current flows between the nonmagnetic titanium/gold (Ti/Au) reference contact and the fluorographene/MgO/Py/Au ferromagnetic tunneling contact as shown on the left side of the device. A non-local voltage measured due to a pure spin current is then measured between a second set of similar contacts on the right of the device. **(b)** In this illustration, the fluorographene/MgO/Py/Au contacts are different widths to exploit shape anisotropy, allowing the magnetic moments in the contacts to switch at different fields, leading to the resistance states seen in the inset of **(c)** where the green arrows indicate a low/high magnitude resistance state when the relative magnetic moment orientations are parallel/antiparallel. The black/red curve in the inset is for sweeping the magnetic field from negative/positive to positive/negative. The magnitude of the resistance change is measured as ΔR_{NL}. The inset is at room temperature as indicated in the large curve of **(c).**

as a chemical diffusion barrier to prevent oxidation and unwanted alloying. Additionally, it can be grown in large area sheets inexpensively in a simple furnace reactor [10]. When graphene is exposed to xenon difluoride (XeF_2) gas, the fluorine ions bond to the graphene surface to create fluorographene. This layer is completely insulating and serves as an atomically thin barrier between the FM and the spin channel.

As a charge current passes from a FM contact, through the tunnel barrier, into the Cd_3As_2 channel and out of a reference contact [titanium/gold (Ti/Au)], a spin current is also produced that radiates outward. Because the spin current travels in all directions, unlike the charge current, it is detected in the second set of FM/Au contacts. The measured electrical resistance at the second FM will be higher when the magnetic moments of the two FMs are antiparallel compared to when they are parallel, giving the HIGH and LOW states necessary for digital memory. The magnetic moments are switched using an external magnet as described in the caption of figure 4. Alternatively, the spin current simply toggles on and off by decreasing the spin relaxation time in the channel using, for example, a gate voltage, allowing logic operations with the same device.

Recently we demonstrated high-quality spintronic switching in a Cd_3As_2/graphene NLSV heterostructure device from cryogenic temperatures up to room temperature. Our devices, the first NLSVs to utilize Cd_3As_2, operate with a 10 times larger signal than silicon-based devices. Moreover, this is just the first step. Our ongoing research includes controlling the quantum phase of the Cd_3As_2 in the device by changing the channel thickness, applying an electric field through external gating, or atomically doping the Cd_3As_2 films.

Metamagnetic iron rhodium

Another possible way to improve spintronic switching behavior and realize next-generation topologically enabled logic or memory elements is to incorporate ferromagnets that are more complex with greater functionality and improved material properties. One material of particular interest is FeRh. FeRh possesses a temperature-dependent metamagnetic phase change where it transitions from antiferromagnetic to ferromagnetic (AFM-FM) with increasing temperature [11]. The temperature at which this transition occurs

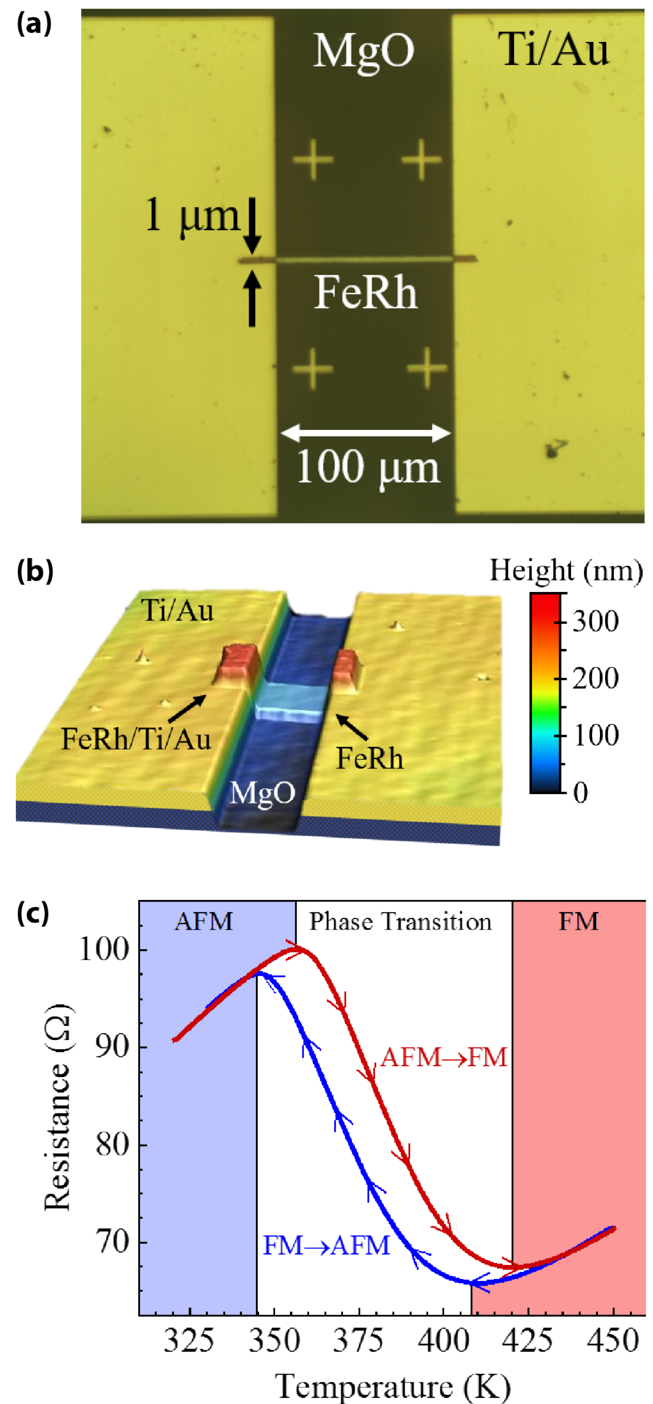


FIGURE 5. (a) This diagram is a top-view optical image of the fabricated device with FeRh wire width and length of 1 micrometer (µm) and 100 µm, respectively, and **(b)** is a 3D optical image of the device. **(c)** This graph shows the resistance measurement while varying the ambient temperature from 320–450 K. Red and blue curves represent heating and cooling cycles, respectively. Background shading colors denote temperature regimes at which the FeRh is antiferromagnetic (AFM, blue), ferromagnetic (FM, red), and in transition (white).

(T_{Cr}), can be fine-tuned using various fabrication techniques, such as substitutional doping [12] and patterning [13]. According to Pouillet's law, expansion of a unit cell will naturally cause its electrical resistance to decrease for a given length of material. Therefore, by careful manipulation of temperature, both the magnetic state and electrical resistance can be selected, allowing its use in switching device applications. This becomes even more attractive when considering the 350 femtosecond AFM-FM transition time, translating to an operating frequency of nearly 3 terahertz [14].

Optical images of simple FeRh devices that we fabricated by standard lithographic methods are shown in figures 5(a) and (b). The simplicity of fabrication is another advantage of working with FeRh. Figure 5(c) demonstrates the AFM-FM transition. The measurement begins at a starting temperature of 320 kelvins (K). Upon increasing the temperature (red curve), the wire resistance also increases. The AFM-FM transition begins once the FeRh temperature surpasses 365 K, accompanied by a decreasing resistance. The effect persists until the temperature reaches 420 K, indicating that the wire has fully transitioned into the ferromagnetic phase. The opposite effect occurs when cooling the wire (blue curve).

To make a useful device, the state must be controlled via current rather than temperature. According to the Joule-Lenz law, an electrical current through the wire will cause the FeRh temperature to increase until it thermally stabilizes. In figure 6(a), a pulsed current controls the temperature. The FeRh temperature and subsequent resistance are held to a constant value by a constant current (I_{Read}). Here, the FeRh will remain in the high-resistance AFM phase (OFF state). If the current amplitude is sufficiently increased, the wire temperature will rise past T_{Cr} and the FeRh will transition into the low-resistance ferromagnetic phase (ON state). As shown previously, the FeRh will remain in the ferromagnetic phase until cooled to below T_{Cr}. Therefore, applying a continuous current (I_{Read}) will maintain the present state of the device. Upon reducing the current, the FeRh transitions back into the high-resistance antiferromagnetic phase (OFF state). In figure 6(b), a pulsed current switches the FeRh back-and-forth between antiferromagnetic (OFF) and ferromagnetic (ON) states.

One possible application of a device with this hysteretic behavior is as a memristor, the basic memory component of many neuromorphic circuit designs. The device demonstrated here uses the magnetization

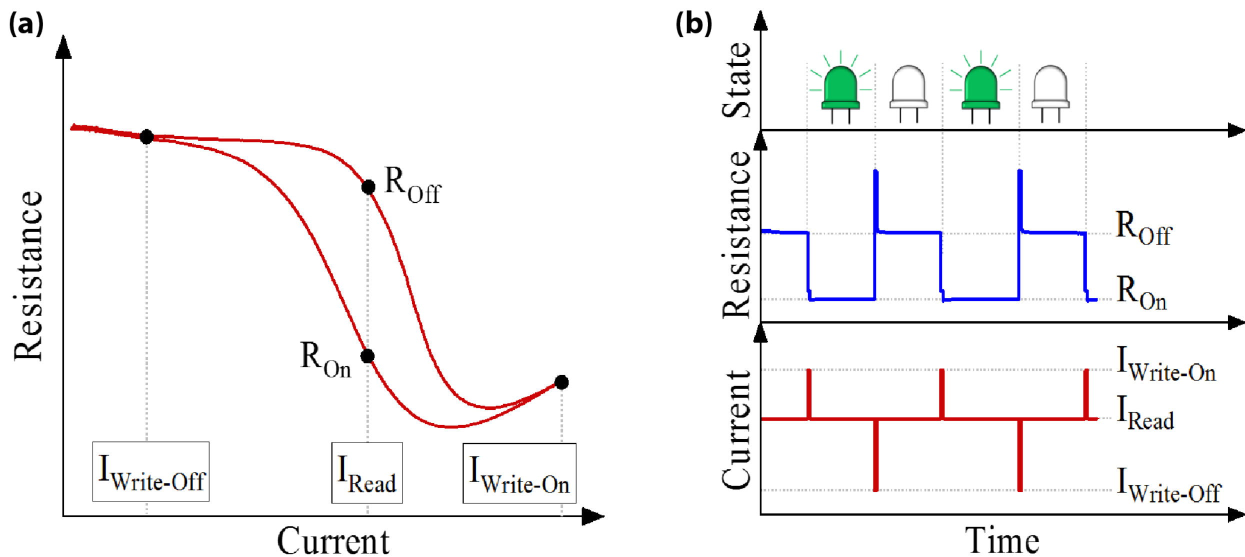


FIGURE 6. (a) This graph shows FeRh resistance as a function of current. Joule heating changes the wire temperature and subsequent phase, allowing for antiferromagnetic and ferromagnetic state control via electrical bias. A constant current I_{Read} will allow the FeRh temperature to stabilize. An FeRh transition is made with a short current pulse of $I_{Write-Off}$ or $I_{Write-On}$. **(b)** This graph shows the resistance and current profiles as a function of time. Repetitively switching between pulse current amplitudes of $I_{Write-On}$ and $I_{Write-Off}$ causes FeRh phase transitions and substantial change in the wire resistance. The green bulbs represent the ON state.

of the material as a state variable, which inherently provides reproducibility, endurance, and state retention in comparison to charge-based switching devices. The switching capability of these devices is estimated to be on the order of 1 picosecond [14]. For comparison, previously reported devices with more advanced architectures have switching times that range from 50 nanoseconds to more than 100 microseconds [15, 16]. Moreover, one could imagine incorporating a metamagnetic element into the previously described NLSV. The metamagnetic transition would switch off the spin current in the NLSV, thereby allowing transistor-like behavior. Alternatively, the metamagnetic transition could switch the device into a new operational mode.

Conclusion and a beginning: Vision for the future

Moore's law began as an observation of the density of transistors in a circuit. Serving as a roadmap for the entire semiconductor industry, it has subsequently transformed into a self-fulfilling prophecy. It has been re-imagined, re-invented, and ultimately embraced as a mindset, an approach, and a philosophy. Device scientists and engineers have accomplished everything envisioned by Gordon Moore in 1965 [17] and are quickly approaching the physical limits which portend an end to this path.

One possible path toward a new scientific paradigm can be found by going back in history to even before the 1965 observation by Moore. Richard Feynman, in his famous speech "There's plenty of room at the bottom" [18], given at the American Physical Society meeting in December 1959, is often credited with inventing the field of nanoscience. He revisited and repurposed a similar line of reasoning in a 1983 speech given at the Jet Propulsion Laboratory and, astonishingly, established the field of quantum computing [19]. Although his prophesies do not specify a pathway to advanced classical HPC, Feynman does establish a way forward by suggesting a holistic, outward-looking approach to device (co-)design. Summarizing this approach, Feynman said, "It would be interesting in surgery if you could swallow the surgeon" [18].

The novel materials and devices that we described here present the beginning of a new era in computing technologies. In his address to the American Physical Society, Feynman said:

> What could we do with layered structures with just the right layers? What would the properties of materials be if we could really arrange the atoms the way we want them?... I can't see exactly what would happen, but I can hardly doubt that when we have some control of the arrangement of things on a small scale we will get an enormously greater range of possible properties that substances can have, and of different things that we can do.

Indeed, by choosing the best materials and combining them in new ways with operating modes in mind, we can optimize our future computing systems and maintain a critical quantitative edge for the future.

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